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Studying Impact of Various Leakage Current Reduction Techniques on Different D-Flip Flop Architectures

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ABSTRACT

In the present scenario the technology is getting finer. Hence there is an aggressive scaling of CMOS device and abbreviates the device density. Lowering the supply voltage leads to lower threshold voltage and oxide thickness. High device density and lower threshold voltage result in significant increase in the leakage power dissipation. It cannot be neglected anymore. This fact has motivated a lot of researchers and technologists to choose leakage current minimization techniques. Therefore it is necessary to reduce leakage power of portable battery operated devices. The main objective of this paper is study of existing leakage current reduction techniques and different D Flip-Flop architectures, and comparing them in terms of ability to reduce leakage and their associated delay overhead. The further approach is to combine different leakage reduction techniques in a single design. Extensive SPICE simulation results were reported using 16nm process technologies.

Keywords : DFF, Leakage current, CMOS stacking.

1 INTRODUCTION

Swift growth in semiconductor technology has led to shrinking of features size of transistor. This has allowed for a large circuits with complex functionality fabricated on a single chip to achieve higher density, performance and lower power dissipation in order to abbreviate the CMOS technology feature size. As per this technology trend, transistor leakage power has increased exponentially. The modern portable battery operated devices such as, cell phones, laptops; PDAs are affected by high power dissipation. Due to this power dissipation, the battery life is reduced. However there is no way to neglect tradeoff between power, delay and area. That's why the designers are required to choose appropriate leakage current reduction techniques.

Power consumption of CMOS consists of dynamic and static power. The main function of dynamic power is to charging and discharging of load capacitance at an average frequency over any given interval time. An effective power technique to reduce dynamic power dissipation is supply voltage scaling. Thus in deep sub micron process (DSM) we lower the supply voltage in order to increase the leakage power. There are various techniques to reduce the static power dissipation.

The remaining of the paper is organized as follows: Section II describes sources of leakage current in DSM. This is followed by previous work regarding existing various leakage current reduction techniques in section III and different D Flip-Flop architectures in section IV. Section V proposes techniques such as, LECTORMTSTACK and LECTORSCSTACK. Simulation procedure and results are provided and also comparison of results is given in section VI. Section VII concludes this work [1],[2]

Leakage current is mainly due to reduction in $V_{th,}$ oxide thickness and channel length. Among the sources of leakage current this project mainly concentrates on sub threshold leakage current.

2 SOURCES OF LEAKAGE CURRENT

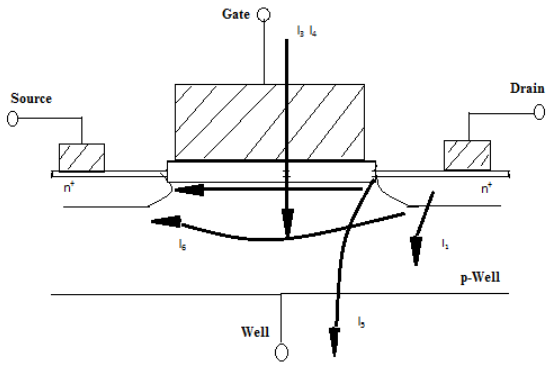

Figure 1: Leakage current mechanism of deep sub micron transistors

In Figure 1, I1 is the reverse-bias p-n junction leakage current, I2 is the sub threshold leakage current and I3 denotes the oxide tunnelling current. I4 is the gate current due to hot-carrier injection and I5 is the Gate- induced drain leakage current. I6 indicates the channel punch through current.

The sub threshold leakage current is the current that flows between the source and the drain of a MOSFET when transistor is operated in sub $V_{th,}$ due to a weak inversion layer [1].

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3 Existing Circuit Level Leakage Reduction Techniques

The static power CMOS circuit is determined by the leakage current through the transistor. To suppress the power consumption in low voltage circuit, it is necessary to reduce the leakage power in both active and standby modes of operation. Standby leakage current is the current flow through the circuit when the circuit is in idle state. Active leakage current flow occurs, when the device is in use

Some of the already proposed leakage current reduction techniques are:

3.1 Power Gating Techniques

3.1.1 MTCMOS techniques:

The Multi Threshold technique is the combination of both high V_{th} and low $V_{th.}$ The high V_{th} prevents sub threshold leakage in standby mode. The low V_{th} has high operating speed with small propagation delay [1] – [5].

3.1.2 SCCMOS techniques:

Super Cut off CMOS is an alternate to MTCMOS. In this scheme the sleep transistor are under driven (OR over driven) when in standby mode [3] –[4].

3.2 Forced Transistor stacking (FTS)

Stacking of transistor is an effective way to reduce leakage current in active mode. A single transistor of width W is replaced by two transistors each of width W/2. Reduction in leakage current takes place when multiple transistors are turned off. This is known as, "Stacking Effect (or) Self Reverse bias effect". The transistor stacking technique depends upon the source voltage V_s. Thus the sub threshold leakage current reduces exponentially [1]-[2], [7].

3.3 Sleepy Stack (SS)

The sleepy stack approach has a combination of both sleep and stack approach. Place a sleep transistor in parallel with one of the stacked transistors. The stacked transistor suppresses the leakage current and sleep transistor are placed parallel to one of the stacked transistors. It reduces the resistance path from V_{dd} to gnd. So the delay is reduced during active mode [6].

3.4 Multi Threshold Stacking (MTSTACK)

It is a combination MTCMOS and FTS. During standby mode, multiple transistors connected in series are turned off and it saves leakage power. In Active mode with high V_{th}, stacked transistors are turned on, hence normal operation of the circuit occurs [11].

3.5 Super Cut off Stacking (SCSTACK)

It is a combination of SCCMOS and FTS. To stack the sleep transistor are under driven (OR over driven) condition. It reduces the leakage current when the multiple sleep transistor connected in series are turned off [11].

3.6 Lector

This technique introduce two transistors [PMOS and NMOS] called leakage control transistors (LCTs) which are inserted in series between pull-up and pull-down network. In the two transistors, anyone of the transistor is always cut off for the applied input. This increases the resistance path from V_{dd} to gnd and also decreases the leakage current. The main advantage of Lector technique is that it works in both active and standby mode [4], [9], [10].

4 Different D – Flip Flop Architecture

4.1 True Single Phase Clocking (TSPC)

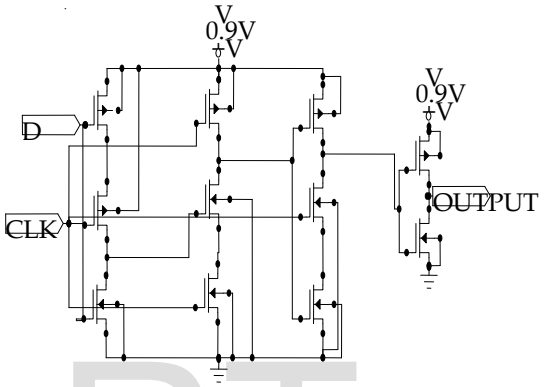

Figure 2: 9 TSPC D – Flip Flop

The Flip-Flop consists of 9 transistors as shown in Figure 2. True Single Phase Clock signals which are never inverted and fit both static and dynamic CMOS circuits are applied. The clocked switching transistors are placed closer to V_{dd}/ ground for higher speed. The state transition of the Flip-Flop occurs at the rising edge of the clock signal. No clock skew exists except the clock delay problems [12], [13].

4.2 NAND Based D – Flip Flop

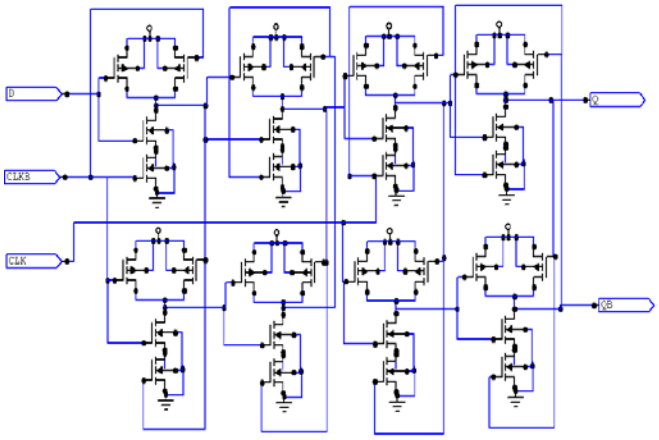

Figure 3: NAND based D – Flip Flop

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It is constructed based on both master and slave latches. In this configuration output of master latch is the input of slave latch and the output of slave is the output of the Flip-Flop. To receive the input data D depending upon the clock signals CLK and CLKB to use the edge of the circuit shown in Figure 3.

5 PROPOSED TECHNIQUES

5.1 Lector Multi Threshold Stacking Techniques

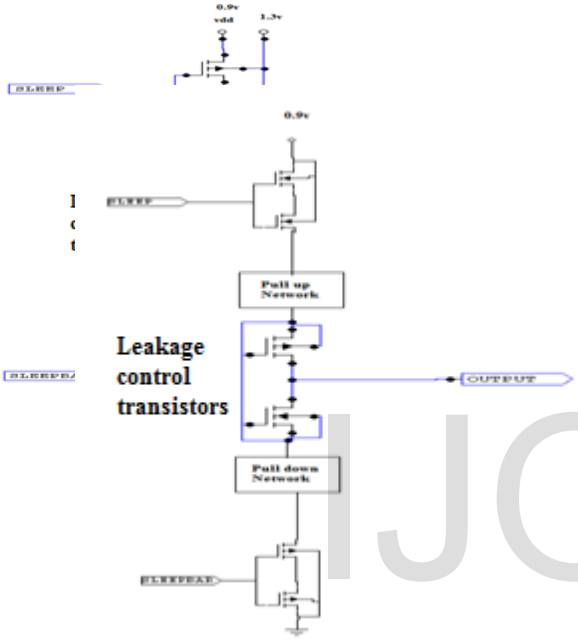

Figure 4: LECTOR Multi Threshold CMOS Stacking

It is a combination of lector and multi threshold stacking techniques as shown in Figure 4. Where the lector technique have leakage control transistor (PMOS and NMOS) if any one of the transistor is always cutoff for whatever input combination is applied. This is increases the resistance path from supply to ground and also reduces the leakage current. The stacked transistor is tuned ON to perform normal operation. If sleep transistor is turned OFF means it creating virtual supply/ground and cutting off the supply. It causing leakage current should be reduced while it maintains high speed in active mode.

5.2 Lector Super Cutoff Stacking Technique (LECTORSCSTACK)

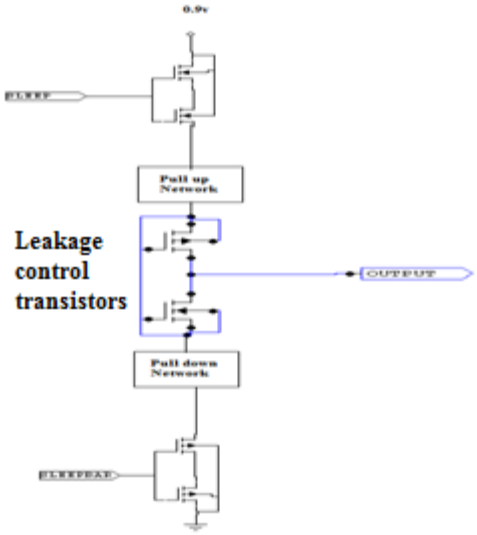

Figure 5: LECTOR Super Cut off CMOS Stacking

It is a combination of lector and super cutoff stacking techniques as shown in Figure 5. During active mode, any one of the LCT is turned on and performs normal operation whereas the LCTS limits the leakage current. In standby mode the stacked transistors which are under driven (or over driven) are turned off. This creates virtual supply/ground rails and cutting off the circuit from supply/ground, causing leakage current reduced by combining of lector and super cutoff stacking.

6 SIMULATION AND RESULTS

Both 9TSPC and NAND based D flip-flop are designed simulated and functionally verified using 16nm CMOS technology files in T-SPICE tool. We have used V_{th} transistors in all designs to show the performance benefits and comparison of different techniques. These techniques are applied to both 9TSPC and NAND-based D flip-flop. Static power for both D flip-flops during active and sleep(idle) mode as well as total (dynamic) power during clocked operation are all measured using T-SPICE tools.

Table 1 provides the static power and total power dissipation for 9TSPC. From the power result, it is observed that proposed technique LECTOR MTSTACK is second most efficient for P_{AVG}. For P_{STATIC}, FTS is the most efficient technique. Where the average power of lector is more leakage when compare to conventional but the static power of lector is efficient than conventional. The proposed techniques are more efficient when compare to lector technique on both average and static power.

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TABLE 1
COMPARISION TABLE FOR TSPC

TECH-NIQUES	P_{AVG} (NW)	P_{STATIC}	DE-LAY	PDP (aJ)	%RE-DUC-TION OF P_{AVG}
Conven-tional	4.29	$2.62X10^{-12}$	0.82	0.0035	-
MTCMOS	2.40	$2.59 X10^{-12}$	1.68	0.0040	44.05
SCCMOS	2.77	$2.09 X10^{-12}$	1.27	0.0035	35.43
FTS	3.78	$6.13 X10^{-13}$	1.2	0.0045	11.88
SS	3.06	$2.54 X10^{-12}$	0.47	0.0014	28.67
MTSTAC K	2.72	$2.70 X10^{-12}$	1.25	0.0034	36.59
SCSTACK	3.27	$2.44 X10^{-12}$	1.69	0.0055	23.77
LECTOR	5.30	$1.68 X10^{-12}$	1.25	0.0066	Nil
LECTOR MTSTAC K	2.55	$2.27 X10^{-12}$	1.26	0.0032	40.55
LECTOR SCSTACK	3.11	$2.46 X10^{-12}$	1.27	0.0039	27.50

TABLE 2
COMPARISION TABLE FOR NAND BASED D FLIP-FLOP

TECH-NIQUES	P_{AVG}	P_{STATIC}	DELAY	PDP (aJ)	%RE DUC TIO N OF P_{AVG}
Conven-tional	$9.15X 10^{-9}$	$5.65X10^{-12}$	1.11	0.0010	-
MTCMOS	$5.37 X10^{-9}$	$5.56X10^{-12}$	1.48	0.0079	41.33
SCCMOS	$4.08 X10^{-9}$	$5.50X10^{-12}$	1.22	0.0049	55.40
FTS	$9.99 X10^{-9}$	$6.13 X10^{-13}$	0.84	0.0083	Nil
SS	$9.82 X10^{-9}$	$2.54 X10^{-12}$	0.84	0.0082	Nil
MTSTAC K	$9.23 X10^{-9}$	$2.70 X10^{-12}$	0.74	0.0068	Nil
SCSTACK	$1.04 X10^{-8}$	$2.44 X10^{-12}$	0.74	0.0076	Nil
LECTOR	$1.17 X10^{-8}$	$1.68 X10^{-12}$	1.11	0.012	Nil
LECTOR MTSTAC K	$1.08 X10^{-8}$	$2.27 X10^{-12}$	1.48	0.015	Nil
LECTOR SCSTACK	$1.05 X10^{-8}$	$2.46 X10^{-12}$	1.425	0.014	

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Table 2 provides information about power dissipation for NAND based D flip-flop. From the power result, it is observed that SCCMOS is efficient for P_{AVG} and for P_{STATIC}, FTS technique is the most efficient. MTSTACK and SCSTACK have low delay. Conventional is efficient for power delay product. MTCMOS only have high percentage to reduces the leakage current all other techniques have less efficient to reduces the leakage current for NAND based D-flip flop.

7 CONCLUSION

Thus the studying impact of various leakage current reduction techniques on different D flip-flop architecture is implemented in 16nm technology. The static power is optimized by using various leakages current reduction techniques. It also proposes hybrid power optimization techniques such as LECTOR MULTITHRESHOLD STACKING and LECTOR SUPER CUTOFF STACKING. If this leakage reduction technique is applied to any of the combinational or sequential circuit, some D flip-flop architecture methods are efficient when compared to other method, which can be used for future work.

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REFERENCES

[1] Kaushik Roy, Saibal Mukhopadhyay and Hamid Mahmoodi-Meimand, Leakage current mechanisms and Leakage current reduction techniques in Deep Sub Micrometer CMOS Circuits, in Proceedings oh IEEE, Vol-91, No-2, 2003

[2] B.S. Deepaksubramanyan and Adrian Nu˜nez EECS Department, Syracuse University , Analysis of Sub threshold Leakage Reduction in CMOS Digital Circuits, Proceeding of the 13TH NASA VLSI Symposium Post Fall, IDA-HO, USA, June 2007.

[3] Kawaguchi, H., Nose, K., and Sakurai, T. " A Super Cut-Off CMOS(SCCMOS) Scheme for 0.5-V Supply Voltage with Pico ampere Stand-By Current," IEEE Journal of Solid State Circuits vol.35,n.10 pp.1498-1501, October 2000.

[4] Deshmukh, Kavita khare," Implementation and Analysis of SC-LECTOR CMOS Circuit Using Cadence Tool", International Journal of Engineering Science and Technology Vol. 2(5), pp 1250-1252.

[5] Anup Jalan and Mamta Khosla," Analysis of Leakage Power Reduction Techniques in Digital Circuits".

[6] P.Srikanth "Design of Ultra-low Leakage Power Sequential Circuits" Vol 3 (3), IJCTA MAY-JUNE 2012.

[7] M.Janaki Rani and Malarkann," Leakage Power Reduction and Analysis of CMOS Sequential Circuits," International Journal of VLSI design & communication system(VLSICS) Vol.3, No.1,February 2012.

[8] Uma nirmal "A Low power high speed addressing using MTCMOS techniques" IJCEM International Journal of Computational Engineering & Management, Vol. 13, July 2011.

[9] Archana nagda, Rajendra Prasad, Trailokya nath sasamal,N.K Vyas," Leakage Power Reduction Techniques:A New Approach" International Journal of Engineering Research and Application(IJERA) ISSN: 2248-9622 Vol. 2 Issue 2, Mar-Apr 2012, pp.308-312.

[10] Rajani H.P and S.Y Kulkarni," LSPR: Novel Low Power State Reduction Technique for CMOS VlSI Design" International Journal of Computer Application (0975-8887) Vol.51, No.18, August 2012.

[11] R. Udaiyakumar and K. Sankaranarayanan," Dual Threshold Transistor Stacking (DTTS) - A Novel Technique for Static Power Reduction in Nano scale Cmos Circuits" European Journal of Scientific Research ISSN 1450-216X Vol.72 No.2 (2012), pp. 184-194 © EuroJournals Publishing, Inc. 2012.

[12] R.Uma, " Flip-Flop Circuit Families:Comparison of Layout and Topology for Low Power VLSI Circuits," International Journal of Engineering Research and Applications (IJERA) Vol. 1, Issue 4, pp.1971-1982.

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