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MIL-STD-1553 BUS PROTOCOLS IP CORE IMPLEMENTATION IN FPGA TO REALISE SYSTEM-ON-CHIP (SOC) :TESTING, VALIDATION & ANALYSIS

K. Padmanabham[1], Prabhakar Kanugo[2], Dr.M. Chandrashekar[3], Dr.K. Nagabhushan Raju[4]

[1,]Analogic Controls India Ltd – Hyderabad-.[1,] E-mail: kpadmanabham7@gmail.com
[2],Analogic Controls India Ltd – Hyderabad, . [2]E-mail: kpkar@analogiccontrols.com
[3]Bharat Dynamics Limited, Hyderabad, India, [3]E-mail: cmatham@gmail.cpm
[4]Dept of Electronics, SK Univ., Ananthpur, India, [4]E-mail:knrbhushan@yahoo.com,

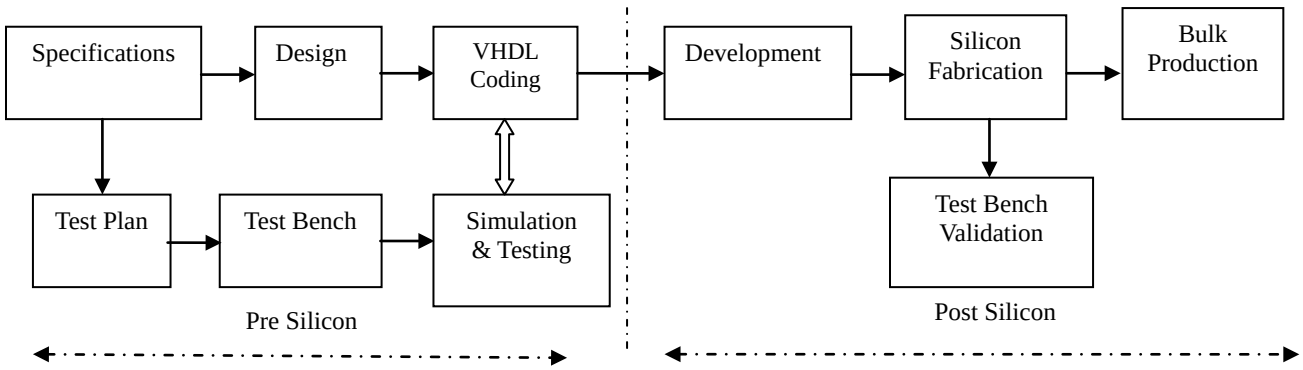
ABSTRACT
The advancement of technology in the area of System-On-Chip (SoC) and IP core, opens new scope for industry to develop their own products, specific to the application with high efficient at low cost. Author [1] discussed the development of SoC with MIL-STd-1553B protocol IP Core and proposed protocol algorithms of MIL-STD-1553B for avionics communication bus, which are protoble in a single FPGA to realize SoC or can go for SoC silicon fabrication. The present paper discusses the testing and validation of 1553 bus protocol IPCore and presents a case study of the "BC to RT protocol" IP Core through "FPGA prototype methodolgy". The proposed schemes have cost advantages, Low foot print, Low cost and increased processing power to handle the applications also.

Keywords: System-On-Chip (SoC), FPGA, MIL-STD-1553B, Protocols, IP-Core, command word(CW), Status word(SW), Data word (DW), FPGA Prototyping, VHDL and Algorithms

Introduction:
The full fledged "System-On-Chip" will have the MIL-STD-1553B bus protocols IP Core, Supervisory processor IP Core, Memory, Manchester Encoding, Manchester Decoding, External interfaces.

The SoC requires a testing and validation schems before FPGA porting or SoC silicon fabrication. The silicon fabrication of SOCs is costly and to control or achieve success at the first fabrication, it is important to ensure the correctness of the IP Core design in terms of hardware & software. The IP core design must undergo a comprehensive verification, and usi- testing and validation with an affordable hardware platform representing the SoC.The validation of SoC can be "Pre Silicon" stage and "Post Silicon" as shown in Figure-1.It is preferred to go for pre Silicon validation to avoid multiple silicon fabrications. The Pre Silicon validation can be done in several methods, like RTL Simulation, Hardware Acceleration, Emulation and FPGA based Prototyping etc, however the validation by **"FPGA Prototyping"** have key benefits like Low cost, High performance, Easy to test application software also it can be easily deployable and portable in the field for demonstration and testing.
The custom built IP Core of "BC to RT", Manchester Encoding and Manchester Decoding are implemented in the FPGA. These codes are tested by simulation tools and synthesized using the Xilinx tool before porting into FPGA.

Fig-1: System-on-Chip validation schemes



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FPGA prototyping:

The FPGA Prototyping is a single prototyping platform which can verify the hardware, software, application software and ensure the design functionalities before the silicon fabrication of SoC.

The Synthesized VHDL code of the protocols of "BC to RT", Manchester Encoding and Manchester Decoding are generated, Ported into FPGA using Xilinx VIVADO Design Suite. The "FPGA Prototype board" is shown in Figure-2.

Fig-2 : FPGA Proto

Prototype board testing:

The FPGA Prototype board is cleared by Boundary scan and connected in the test set-up shown in Figure-3. The test set-up equipments are:

- FPGA Prototype card is loaded with VHDL code for the "BC to RT Protocol".
- LAPTOP is to issue the instructions to the FPGA Prototype card.
- DDC make RT Module is used as Reference RT to respond and send Status to BC
- Power Supply is a DC power source for FPGA
- Oscilloscope is used for capturing the 1553 waveforms and storing.

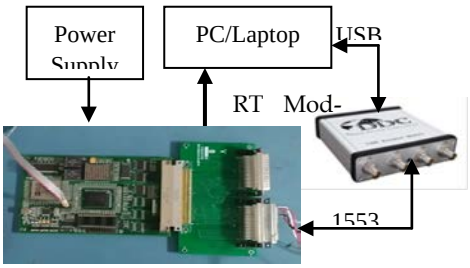
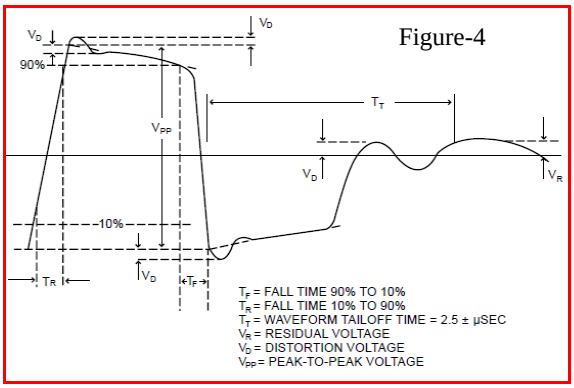


Figure 3 : FPGA Functional Test set-

1553 bus Signals validation:

The FPGA Prototype card is ported with the BC to RT Protocol to perform as "Bus Controller (BC). The DDC make RT module is used as a reference terminal for validating the commands from the BC. The communication from BC to RT and response from the RT to be verified, simultaniously 1553 waveforms on the bus will to be captured on the oscilloscope for waveform verification.

The standarde 1553 waveform is depicted as Figure-4 for reference.



1553 bus waveform and Protocols tests:

The tests to be performed on the 1553 bus output from the BC, for validation are categorized into two types: (A) Electrical tests and (B) Protocol Tests.

The "Electrical tests" are related to 1553 waveform "Timing and Amplitude". The "Protocol Tests" are related to the correctness of the Protocols between the BC and the reference RT module. These commands will be repeated multiple times to ensure the reliability and repeatability. It implies the validation is by two independent verifications i.e First by 1553 waveform verification and second is by reference RT module response to the commands from BC.

The Summary of tests to be performed are:

Electrical test measurements on the 1553 waveform

1. Bit time and word time
2. Sync bits for Command, Data & Status
3. Parity bit time
4. Amplitude (V_{PP})
5. Rise-time (T_R)
6. Fall-time (T_F)
7. Zero crossing stability
8. Distortion Voltage (V_D)
9. Output symmetry (V_R & T_T)
10. Terminal response time
11. Frequency stability
12. Inter message time gap
13. Transmission rate

Protocol test to be performed are:

14. BC issuing Command word with data word
15. RT response and Status word

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16. BC Command word Plus 32 data words
17. RT response and Status word

Testing and Results:

The test set-up for conducting the tests, shown in Figure-3. A CW message from BC to RT is initiated and the waveform is captured on the Scope for for measurements. The parameters to be measured are Bit time, Word length, Three Sync waveforms, and Parity bit.

The CW message waveform captured is shown in Figure-5.

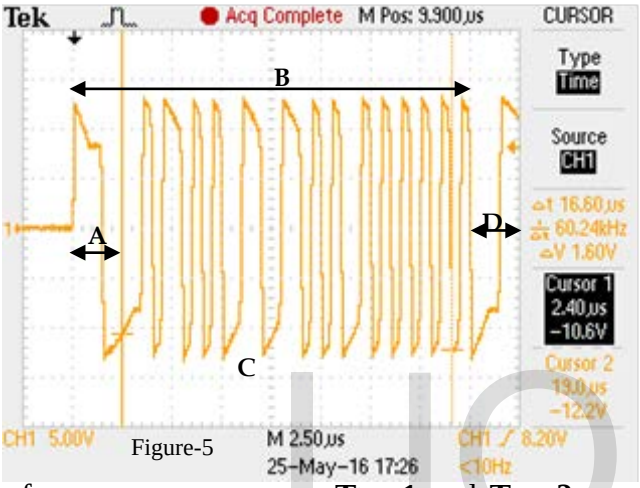

Figure-5

The four parameters as per **Test-1** and **Test-2** measured and tabulated in Table-1

Table-1			
S.No	Parameters	1553 Standards	Measured
A	Command Sync	3µsec	3µsec
B	Word length	20µsec	20µsec
C	Bit time	1µsec	1µsec
D	Data Sync	3µsec	3µsec

The Four parameters measured from the CW waveform are compared with the standards and found meeting the MIL-STD-1553 standards.

The SW response from RT for the CW received from BC is captured and shown in Figure-6

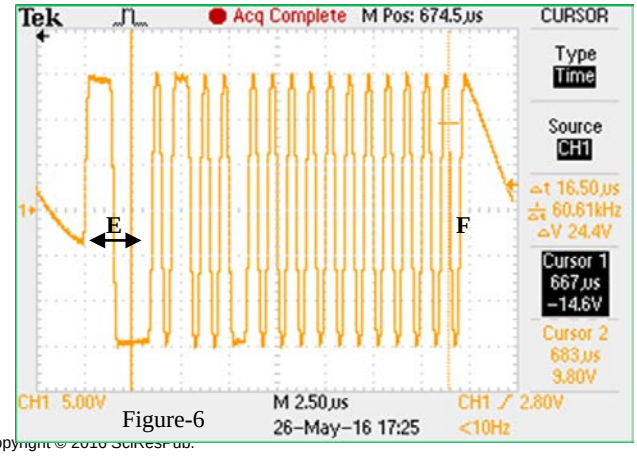

Figure-6

Two parameters measured as per **Test-2** and **Test-3**,are tabulated in Table-2.

Table-2			
S.No	Parameters	1553 Standards	Measured
E	Status Sync	3µsec	3µsec
F	Parity Bit	20µsec	20µsec

Two parameters as shown in Table-2 are meeting the MIL-STD-1553 standards.

Test-4: "Amplitude measurement (V_{pp})" of the waveform is measured on the CW waveform, peak-to-peak voltage as shown in Figure-7. The measured value V_{pp} is 26Vdc and the standard says the acceptable range is 18 to 28Vdc peak to peak.

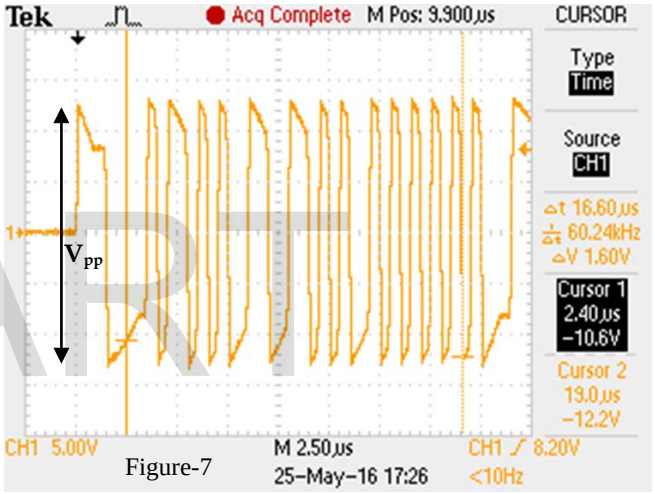

Figure-7

Test-5: "Rise time (T_R)" of the waveform to be measured on the Data Sync waveform, on the rising edge from –ve to +ve at 10% and 90% of the peak-to-peak amplitude. The waveform in the Figure-8, is marked at 10% as V_{10} & 90% as V_{90} on the rising edge and the corresponding timings T_1 & T_2 also marked. The Rise-time (T_R) is time difference between T_1&T_2, which is 140nsec, the standard says 100nsec $\leq T_R \leq$300nsec.

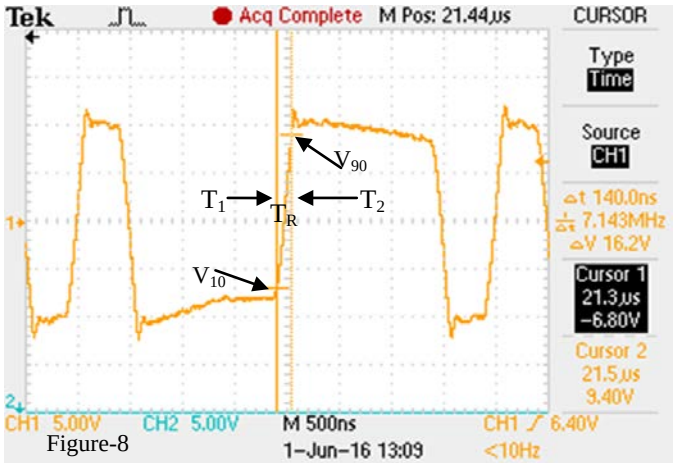

Figure-8

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Test-6: "Fall time (T_F)" of the waveform to be measured on the CW Sync waveform, on the falling edge from +ve to –ve at 90% and 10% of the peak-to-peak amplitude. The waveform in the Figure-9, is marked at 90% as V_{90} & 10% as V_{10} on the falling edge and the corresponding timings T_1 & T_2 also marked. The Fall-time (T_F) is time difference between T_1&T_2, which is 140nsec, the standard says 100nsec ≤ T_F ≤300nsec.

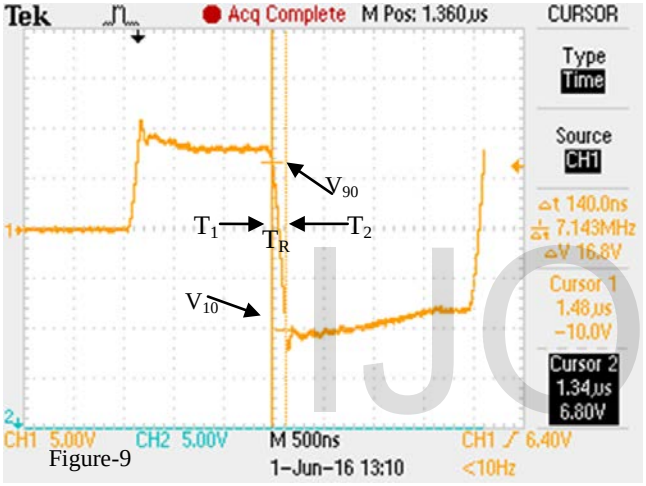

Figure-9

Test-7: The **"**Zero crossing stability" measurements performed on the CW Sync waveform. The 1553 signal waveform marked with the three zero crossing timings i.e T_1, T_2 & T_3, as indicated in the Figure-10. The measuring pulse width are "positive (t_{zcp})" and the "negative (t_{zcn})". The expected Pulse widths are 500 ±25ns. The time between the three zero crossings i.e Pulse widths are t_{zcp} = 500nsec & t_{zcn} = 520nsec.

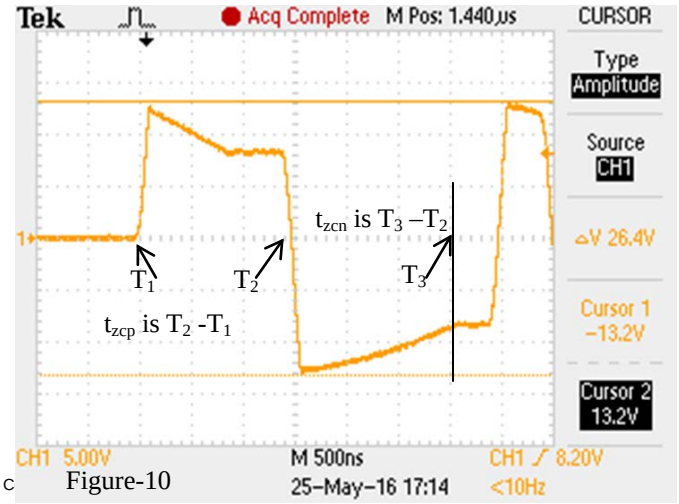

Figure-10

Test-8: The "Distortion Voltage (V_D)" of the waveform i.e V_D, is shown in Figure-4. The acceptable V_D is ± 900 mV peak i.e 1.8V peak-to-peak. The waveform shown in Figure-11, is captured on the oscillo

scope and reproduced from the excel data to expand the related portion of the graph for measurement. The measured value of V_D is 800mV peak-to-peak.

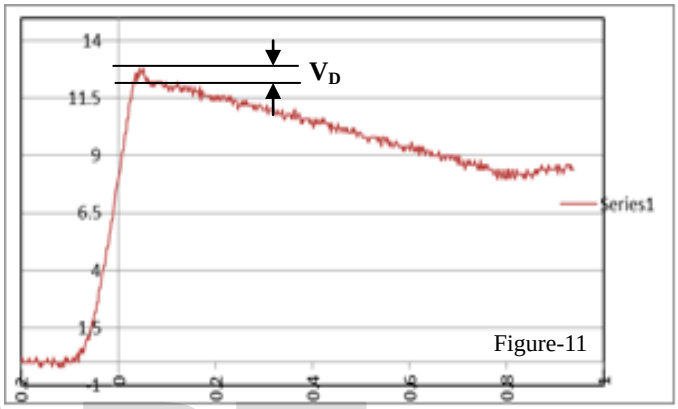

Figure-11

Test-9: The"Output symmetry (V_R & T_T)" is the symmetry of the waveform at the end of each message. The symentry is the defined by the voltage level called "Residual Voltage (V_R)" at the "Tail of time (T_T)" at 2.5µsec from the zero crossing of the parity bit. The acceptable residual voltage V_R is ≤± 250 mV. The waveform shown in Figure-12, is captured on the oscilloscope and reproduced from the excel data to expand the related portion of the graph for measurement. The measured Residual Voltage level at the Tail-off time is ± 200mV. The voltage is with in the acceptable level.

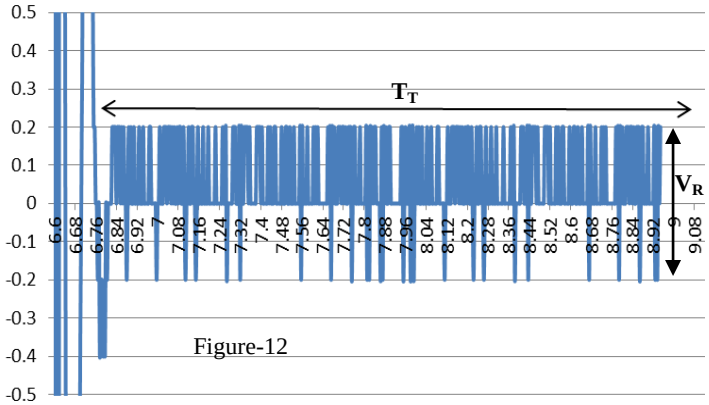

Figure-12

Test-10: The "Terminal Response Time" is the reac-

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tion time of the RT for the messages or commands from BC. The 1553 standard says the response time is to be between 4 to 12µsec.

The waveform shown in figure-13 is regenerated from the excel data of the Ocilloscope captured from the BC command with 32 words to RT and its SW as response.

The measured RT response time is 6.2µsec. which is with in the standard i.e between 4 to 12µsec

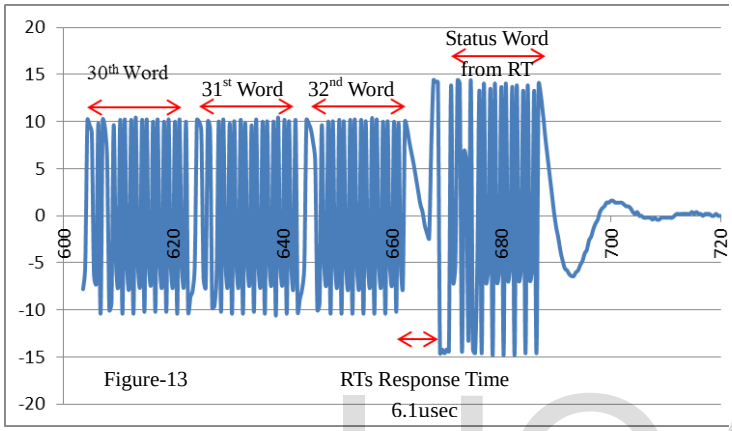

Figure-13

Test-11: The "Frequency stability" of the 1553 waveform is to be less than 0.01%. The frequency of the 1553 waveform is 1MHz selected to achieve 1µsec bit time and 20µsec word length. The frequency measurements are carried out on the output 1553 waveform by capturing on the oscilloscope and measuring the "Bit time" of the data words to compute the frequency. Five measurements were carried out and the observations are tabulated in Table-3. The % of computation for the stability is 100x(Fav-Fmin)/Fav and 100x(Fmax-Fav)/Fav

Table-3: Frequency Measurements

F1	0.99999	Fmin
F2	0.99909	
F3	1.00009	
F4	0.99999	
F5	1.00019	
F6	1.000009	Fmax

The minimum frequency measured is, Fmin = 0.99999MHz and the Fmx = 1.000009MHz. The average Frequency is computed from the above six reading is Fav = 0.999893Mhz.

The Frequency Stability for the

- Min.frequency is 100*(Fav-Fmin)/Fav is 0.00968%
- Max.frequency is 100*(Fmax-Fav)/Fav is 0.11585%

The frequency stability is mainly dependent on the stability of the Internal Oscillator. In this case the oscillator stability is 100ppm which resulted around 0.1%, which can be improved by using more accurate crystal.

Test-12: The "Inter message time gap" is the time space between the messages, which is to be maintained for error free communication on the bus with out missing any data packets. The standard say the time gap can be from 4µsec to 12 µsec. To validate the time gap, two consecutive messages are to be sent from BC to RT, if the RT responds with a Status word for all the messages, it implies the communication is successful. This activity is to be repeated multiple times to ensure the reliability. The test was performed by keeping the time gap at minimum level of 4µsec between two messages and transmitted from BC to RT noted the SW from RT and found the communication is successful.

Test-13: The "Transmission rate" is the rate at which the stream of massages transmitted maintaining the proper communication on the bus. The stream of messages to be transmitted with minimum level inter messages time gap for testing. The test with inter message time gap of 4µsec carried out and found the communication was successful. The inter message time gap less than 4µsec is hammepring the communication.

The **Protocol test** to be performed on the BC is to transmit the commands from BC to RT and check the status word from RT for correctness. Set-up blockdiagram is shown in Figure-14.

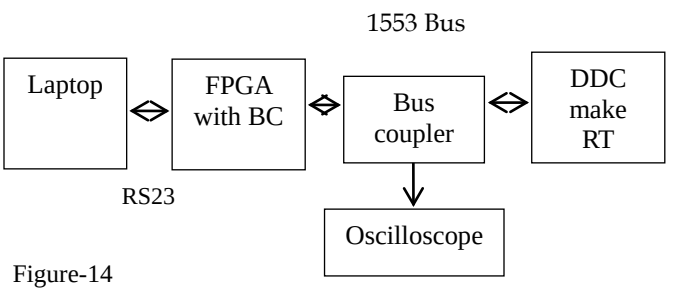

Figure-14

The command & response between the BC and RT will be initiated from the Laptop, simultaneously 1553 waveforms will be captured on the oscilloscope for verification.BC issuing command word to RT with address "00111", the command word pattern is shown in Figure-15 with the expected Manchester waveform. The Manchester waveform is marked from 1 to 17 for comparing with the actual waveform.

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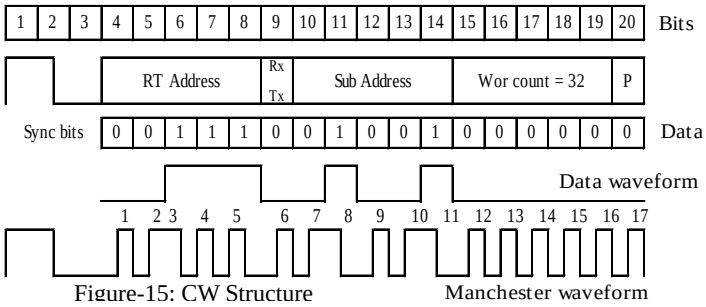

Figure-15: CW Structure

The actual CW waveform is captured and shown in the figure-16. The waveform is marked with from 1 to 17.

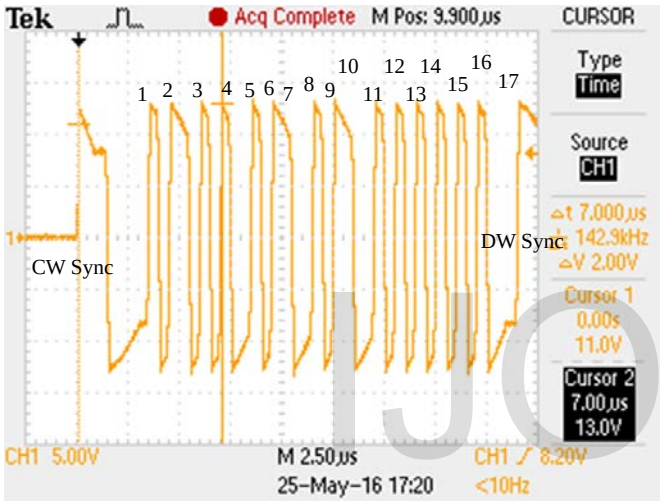

Figure-16: CW 1553 waveform

RT response to the command word is a "Status Word (SW)" and the expected Status word pattern is shown in figure-17 and the actual waveform on the bus is shown in figure-18.

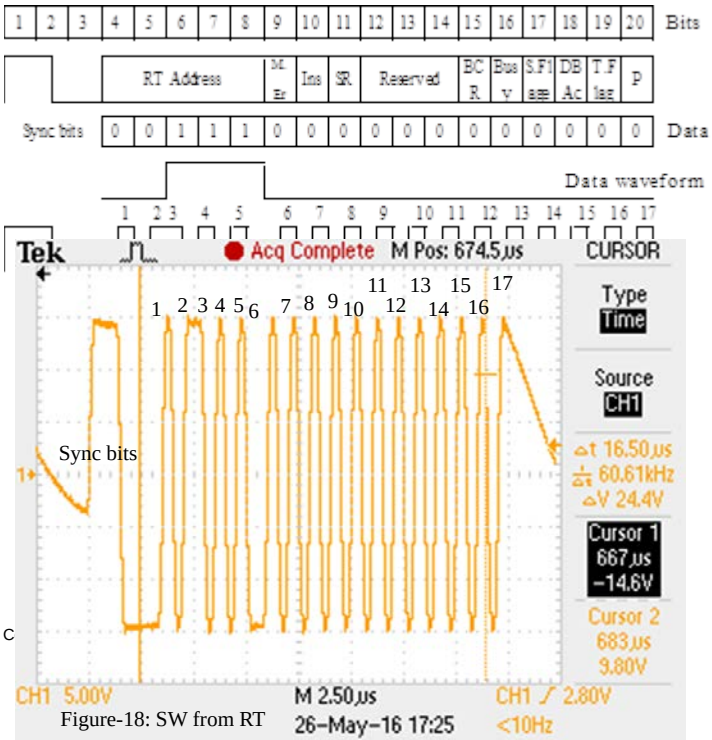

Figure-18: SW from RT

The RT status word actual waveform captured on the scope is shown in figure-18.

The test results are tabulated Table-4 shows the 1553 waveform parameters of the IP Core and the measurements are with in the limits of the 1553 Standards.

Table-4 : Summing up the test results

Test No.	Parameters to be measured	1553 Standards	Results
1	Bit time	1µsec	1µsec
1	Word time	20µsec	20µsec
2	Command Sync	3µsec	3µsec
2	Data Sync	3µsec	3µsec
2	Status Sync	3µsec	3µsec
3	Parity Bit time	1µsec	1µsec
4	Amplitude (V_{PP})	18 to 27Vdc	26Vdc
5	Rise-time (T_R)	≤ 300nsec	140nsec
6	Fall-time (T_F)	≤ 300nsec	140nsec
7	Zero crossing stability	500 ±25ns	500nsec & 520nsec
8	Distortion Voltage (V_D)	± 900 mV Or 1.8V_{pp}	800 mV_{pp}
9	Output symmetry (V_R)	± 250 mV	± 200mV_{pp}
10	Terminal response time	4 to 12µsec	6.1µsec
11	Frequency stability	0.01%	0.01158%
12	Inter message Time Gap	4 µsec to 12µsec	
13	Transmission Rate		

The BC command to Standard RT terminal and its response imply the protocols are working and meeting the MIL-STD-1553B standards.

Conclusions:

The BC to RT IP core implemented in the FPGA proto borad tested as per the MIL-STD-1553 and carried out the electrical mesurements and tested for protocol cor-

rectness by using the reference RT module. At the end all the parameters are meeting the standards except the frequency stability which can be attributed to the stability of the crystal used and can be improved by using more stable in the actual usage. The protocol for all other functions of the 1553 bus to be developed for moving to full fledged SoC for industry usage.

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