Implementation of Embedded Image Registration using FPGA

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Abstract

The main objective of this project work is to implement an image registration algorithm and complementing hardware architecture that can perform the algorithm in real-time and produce accurate results across problem domains and deliver the results in multiple formats to facilitate integration with other embedded image processing systems.

Key words: Image registration, DWT,FPGA

INTRODUCTION

In computer vision, sets of data acquired by sampling the same scene or object at different times, or from different perspectives, will be in different coordinate systems. Image registration is the process of transforming the different sets of data into one coordinate system. Registration is necessary in order to be able to compare or integrate the data obtained from different measurements. Medical image registration often additionally involves *elastic* registration to cope with deformation of the subject (due to breathing, anatomical changes, and so forth). Elastic registration of medical images can also be used to register a patient's data to an anatomical atlas..

FPGA: A field-programmable gate array (FPGA) is an integrated circuit designed to be configured by the customer or designer after manufacturing—hence "field-programmable". The FPGA configuration is generally specified using a hardware description language (HDL), similar to that used for an application-specific integrated circuit (ASIC) (circuit diagrams were previously used to specify the configuration, as they were for ASICs, but this is increasingly rare). FPGAs can be used to implement any logical function that an ASIC could perform. The ability to update the functionality after shipping, partial re-configuration of the portion of the design and the low non-recurring engineering costs relative to an ASIC design (not withstanding the generally higher unit cost), offer advantages for many applications.

FPGAs contain programmable logic components called "logic blocks", and a hierarchy of reconfigurable interconnects that allow the blocks to be "wired together"—somewhat like a one-chip programmable breadboard. Logic blocks can be configured to perform complex combinational functions, or merely simple logic gates like AND and XOR. In most FPGAs, the logic blocks also include memory elements, which may be simple flip-flops or more complete blocks of memory.

Aim of the project Work:

The main aim of this project work is to develop an accurate real-time embedded image registration system that can be used in various problem domains (e.g., wearable computing, robotics, and surveillance) while investigating the natural tradeoffs between throughput, cost, generality, and accuracy. To design such a system, an image registration algorithm and complementing hardware architecture is required to be developed that can perform the algorithm in real-time and produce accurate results across problem domains and deliver the results in multiple formats to facilitate integration with other embedded image processing systems.

Existing System and its Problem:

In problems such as background subtraction, spatiotemporal information is commonly used to estimate the probability density function of each pixel in order to identify regions of interest in the scene, and without a pixel-to-pixel relationship between warped images this method cannot be applied. Tracking of objects found through detection is also complicated by camera motion as the motion of the object and camera are combined.

At times, the spatial information provided by one image is not enough to perform the desired task, this can be remedied through the use of mosaicing, the merging of different images after they have been aligned, which allows for a moving camera to produce an increased field of view of a planar region. A similar problem is to increase the spatial resolution of an image through methods of super-resolution, which commonly use multiple images and image registration to relate them to create an image of finer detail than those provided.

Proposed System

In the proposed system, two image registration algorithms are of specific interest for this task (1) Direct featureless method. The choice of this algorithms is motivated by the overall goal of full projective parameter estimation, while allowing for the more straightforward initial implementation. The large overlap in the algorithms allows for the majority of the architecture to be reused when transitioning between the phases of the project. The solid lines represent high bandwidth pixel data-paths and the dashed lines show low bandwidth control signals.

Scope:

The work of the project will be focused on the design of Image registration technique on FPGA. The design includes different block like homographic transformation, Direct featureless algorithm and Hierarchical model-based motion estimation algorithm. All design need to be verified to ensure that no error in VHDL programming before being simulated. Design process will be described on the methodology chapter. The second scope is to implement the design into FPGA hardware development board. This process is implemented if all designs are correctly verified and simulated using particular software. Implementation includes hardware programming on FPGA or downloading hardware design into FPGA and software programming. Creating test vector program also include in the scope of the project. Test vector is a program developed and is intended as the input interface for user as well as to control data processing performed by the hardware. These computation values should be verified and tested to ensure the correctness of the developed module. Appropriate software is used to compare the computation performed by the FPGA hardware with the software. There are several test performed to the design modules and the test process also will be discuss in the methodology chapter.

Software Requirement specification:

- Windows XP with SP2- Professional Edition
- Minimum Intel Pentium IV Processor, 2 GB RAM, 20 GB HDD,
  CD-ROM
- XILINX-10.1 ISE
- MODEL SIM 6.3C

Hardware Requirement specification:

- Spartan-III-FPGA
- Baseboard
- FPGA-XILINX Spartan III 3E100-5tq144
- Programming Tool

Development Methods

The research work is using the Waterfall lifecycle model for the development of the project. The Waterfall model is an activity centered lifecycle model first developed by Royce.

The approach of the Waterfall model is in a step-by-step way where all the requirements of one activity are completed before the design of the activity is started. The entire project design is broken down into several small tasks in order of precedence and these tasks are designed one by one making sure they work perfectly. Once one of these small tasks is completed another task, which is dependent on the completed task, can be started. Each step after being completed is verified to ensure the task is working, error-free and meeting all the requirements.

The research work chose this lifecycle model for the project primarily for two reasons. First reason being simplicity, by using the Waterfall model the entire project can be broken down into smaller activities which can be converted relatively easily into code and once the entire thing is combined the code for the project can be derived. The second reason is because of the verification step required by the Waterfall model it would be ensured that a task is error free before other tasks that are dependent on it are developed. Thus chances of an error remaining somewhere high up in the task hierarchy are relatively low. Some of the unique features of waterfall model are:It can be implemented for all size projects.It leads to a concrete and clear approach to software development.In this model testing is inherent in every phase.Documentation is produced at every stage of model which is very helpful for people who are involved.

System Architecture

Large systems are always decomposed into sub-systems that provide some related set of services. The initial design process of identifying these sub-systems and establishing a framework for sub-system control and communication is called *Architecture design* and the output of this design process is a description of the *software architecture.*

The architectural design process is concerned with establishing a basic structural framework for a system. It involves identifying the major components of the system and communications between these components. In the following sub-sections we delve into the design aspects and the sub systems involved in this software package.

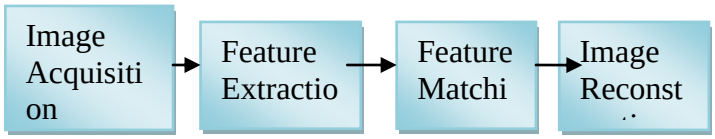
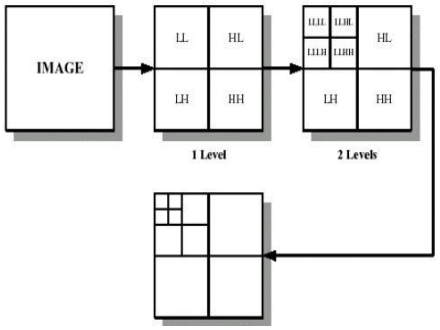


Fig 4.2: Top Level Block diagram for the project.

Detailed Design

mean calculation: average of all pixel in an imageVariance calculation: high level and low level components in an image

2D-DWT:Feature Extraction



Feature Extraction and matching

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jpeg committee has released **its new image coding** standard, jpeg-2000, which has been based upon dwt. the wavelet transform (wt) has gained widespread acceptance in signal processing and image compression. because of their inherent multi-resolution nature, wavelet-coding schemes are especially suitable for applications where scalability and tolerable degradation are important recently the jpeg committee has released its new image coding standard, jpeg-2000, which has been based upon dwt. wavelet transform decomposes a signal into a set of basis functions.these basis functions are called wavelets are obtained from a single prototype wavelet y(t) called mother wavelet by dilations and shifting: where a is the scaling parameter and b is the shifting parameterdiscrete wavelet transform (dwt), which transforms a discrete time signal to a discrete wavelet representation. it converts an input series x0, x1, ..xm, into one high-pass wavelet coefficient series and one low-pass wavelet coefficient series (of length n/2 each) given by:

$$H_i = \sum_{m=0}^{k-1} x_{2i-m} \cdot s_m(z) \qquad (1)$$

$$L_i = \sum_{m=0}^{k-1} x_{2i-m} \cdot t_m(z) \qquad (2)$$

here $s_m(z)$ and $t_m(z)$ are called *wavelet filters*, k is the length of the filter, and i=0, ..., [n/2]-1. in practice, such transformation will be applied recursively on the low-pass series until the desired number of iterations is reached. lifting schema of dwt has been recognized as a faster approach the basic principle is to factorize the polyphase matrix of a wavelet filter into a sequence of alternating upper and lower triangular matrices and a diagonal matrix . this leads to the wavelet implementation by means of banded-matrix multiplications

$$\tilde{P}_1(Z) = \begin{bmatrix} k & 0 \\ 0 & \frac{1}{k} \end{bmatrix} \prod_{i=1}^{m} \begin{bmatrix} 1 & s_i(z) \\ 0 & 1 \end{bmatrix} \begin{bmatrix} 1 & 0 \\ t_i(z) & 1 \end{bmatrix} \qquad (1)$$

$$\tilde{P}_2(Z) = \begin{bmatrix} k & 0 \\ 0 & \frac{1}{k} \end{bmatrix} \prod_{i=1}^{m} \begin{bmatrix} 1 & 0 \\ t_i(z) & 1 \end{bmatrix} \begin{bmatrix} 1 & s_i(z) \\ 0 & 1 \end{bmatrix} \qquad (2)$$

Where $s_i(z)$ (primary lifting steps) and $t_i(z)$ (dual lifting steps) are filters and K is a constant.

Result of DWT:

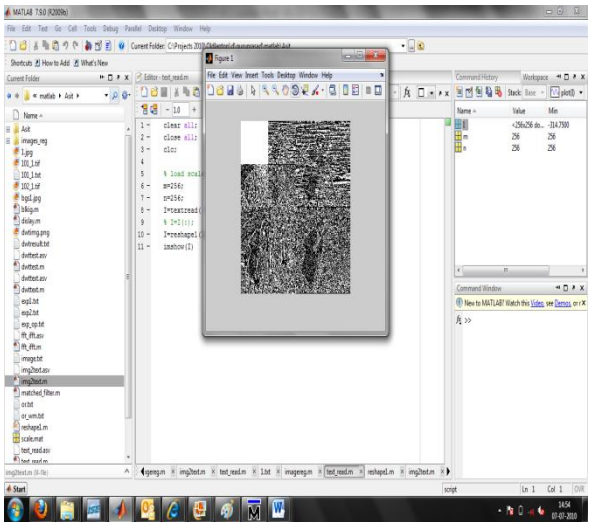
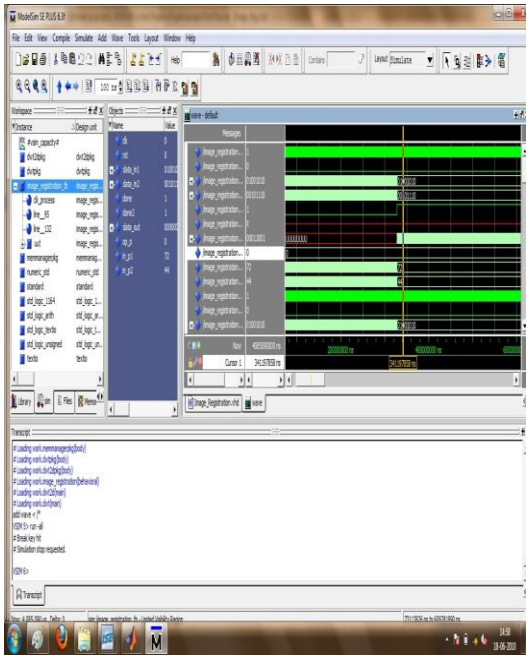
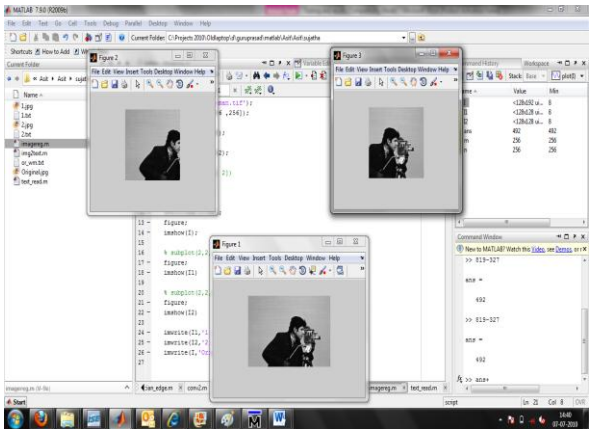


Image shows the DWT of the input image ,we take dwt to obtain different coefficient of the given image like (HH,HL,LL,LH). Out of which we are interested in high level coefficient.



11 Top level waveform for image registration



Conclusion

The work of the project is focused on the design of Image registration technique on FPGA. The design includes different block like homographic transformation, Direct featureless algorithm and Hierarchical model-based motion estimation algorithm. All design is verified to ensure that no error in VHDL programming before being simulated. The second scope is to implement the design into FPGA hardware development board. This process is implemented if all designs are correctly verified and simulated using particular software. Implementation includes hardware programming on FPGA or downloading hardware design into FPGA and software programming. Creating test vector program also include in the scope of the project. Test vector is a program developed and is intended as the input interface for user as well as to control data processing performed by the hardware. These computation values should be verified and tested to ensure the correctness of the developed module. Appropriate software is used to compare the computation performed by the FPGA hardware with the software.

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Author: Jay Brockman, Daniel Rinzler, and Peter Bui