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Behavioural model of Spin Torque Transfer Magnetic Tunnel Junction, Using Verilog-A

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ABSTRACT

A novel simple and efficient model of Spin Torque Transfer Magnetic Tunnel Junction (STT-MTJ) is presented. The model is implemented using Verilog-A. The model accurately emulates the main properties of an STT-MTJ which includes Tunnel Magneto resistance Ratio (TMR), its dependence on the voltage bias and the Critical switching current. The novelty of the model lies in the fact that the voltage dependence of TMR has been modeled using a single equation dividing it into three different operating regions. A register based on the model is also developed. The model can be used for faster simulations of hybrid Magnetic CMOS circuits and in various other wide range of applications. The models were verified using Synopsys Hspice 2010.

Keywords : *Behavioural modeling; Magnetic Tunnel Junction; MTJ; Spin Torque Transfer RAM; Verilog-A*

1 INTRODUCTION

WITH the evolution of supercomputers to handle complex computing tasks there is a requirement of a universal memory [1], as traditional memory technologies like SRAM, DRAM & Flash cannot serve the same purpose due to various limitations like low density in SRAM, Volatility of data in DRAM and Low operation speed & less endurance of Flash [2]&[3]. To serve this purpose and to overcome the limitations in the traditional memory technologies nowadays Spin Torque Transfer Random Access Memory (STT-RAM) is gaining popularity as a future universal memory. STT-RAM promises to provide key features of a universal memory [4] like high density, low cost, high speed, low operation & storage power requirements, random accessibility, non-volatility and unlimited endurance, a memory technology which can handle all the computing requirements of a device.

The basic storage element (Fig. 1) [5] which is used for storage in a magnetic random access memory (MRAM) is a magnetic tunnel junction (MTJ). The basic structure of a MTJ consists of an insulating layer called "tunnel barrier" inserted between two ferromagnetic layers the "free layer" and the "reference layer". The magnetization direction of the reference or the fixed layer remains unchanged and the data is stored by switching the magnetization direction of the free layer. The MTJ is formed by an insulating tunnel barrier sandwiched between two ferromagnetic electrodes (the free layer and the fixed reference layer). The free layer electrode is usually made up of metals such as Fe, Co & Ni and their alloys. The fixed layer is anti-ferromagnetically coupled with the pinned layer through Ru layer to form a SAF (Synthetic Anti Ferro magnet), the pinned layer is further coupled with a anti-ferromagnetic pinning layer [6]. This type of structure makes the free layer easy to write while the fixed layer remains unchanged.

MTJ is the basic building block for the future universal memories, the design of any such system has a great role of computer simulations and the accuracy of the simulation results depends on how accurate device models are used for the simulations. Previously Linda M *et al.* has given a Verilog-A model of a MRAM cell [7] using the Field driven MTJ. Zhao *et al*. created a Verilog-A model of STT-MTJ [8], but the parameters used were related to each other using complex equations and the code was not disclosed in the paper. A circuit base model of STT-MTJ was given by Harms *et al.* [9], but the characteristics of their model cannot perfectly match the experimental data. Lee *et al.*[10] has also given a circuit base model of the STT-MTJ. In this paper a simple and accurate behavioral model of STT-MTJ is presented using Verilog-A, in this model a single equation (Eq. 3.1) is used to show the voltage bias dependence of TMR dividing it into three operating regions that are Parallel region, Anti-parallel region with Positive bias and Anti-parallel region with negative bias. This model can be used for efficient simulations of Hybrid Magnetic CMOS circuits in a faster way.

2 SPIN TORQUE TRANSFER MAGNETIC TUNNEL JUNCTION (STT-MTJ)

The MTJ offers a low resistance when the two layers (Free layer and Reference layer) are magnetized in the same direction, called the "parallel state" and it offers a High resistance when the direction of magnetization of both the layers is op-

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posite, called the "Anti-parallel state", Fig. 1 shows the two states of a MTJ. MRAM bit cell is formed by adding a read transistor (NMOS transistor) in series with the MTJ (Fig.2), the connections to the bit cells are named as bit-line (BL), Source-line (SL) and word-line (WL). The data is read as '1' if the MTJ offers a low resistance and a '0' if the MTJ offers a high resistance or vice versa for negative logic.

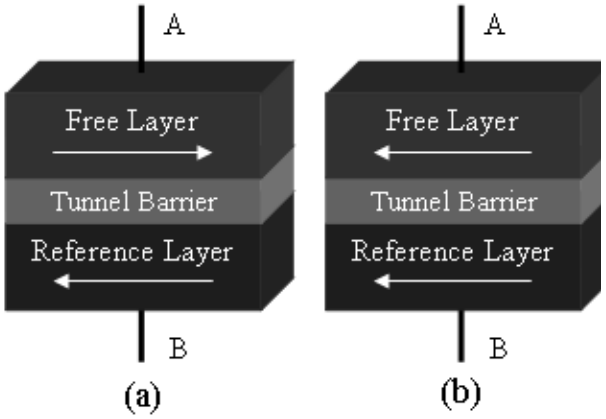

Figure 1. MTJ states (a) Anti-parallel (high resistance) (b) Parallel (Low Resistance).

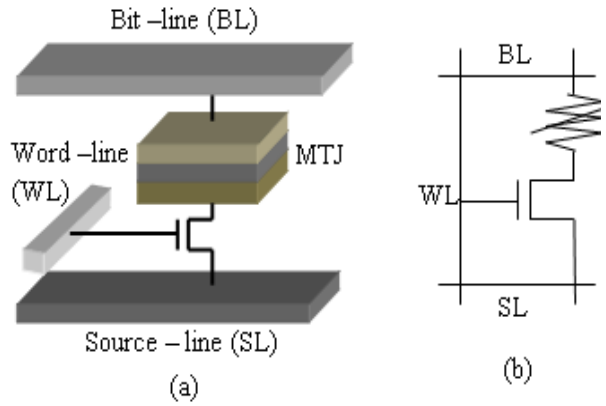

Figure 2. (a) MRAM bit cell (b) Equivalent schematic.

In the first generation of MTJ's the data is written (free layer is toggled) using externally applied magnetic field which is produced using two on chip metal lines. This technique is known as Field Induced Magnetic Switching (FIMS). The data is written on to bit cell by driving a strong electric current through both the metal lines, producing a threshold field at the cross point of the lines. All the other neighboring bit cells are exposed to little more than half the threshold field, which can cause an unwanted overwrite in the neighboring bit cells. This phenomenon is known as the "half select" problem, the most encountered in FIMS technique. To take care of the "half select" problem, the bit cell must be at a proper distance and the threshold must be high so that any external disturbance is unable to change the bit cell. In 1998 it was experimentally shown that high density of spin polarized current can force the ferromagnetic layer to align in a particular direction [10]. STT switching mechanism uses both the preservation of spin direction during electron transit across the spacer and the conservation of angular momentum. The current is spin polarized by adding a polarizing layer as shown in Fig. 3 or by the reference layer itself. The STT-MTJ has a Critical Switching Current (I_c), when I_c is applied on MTJ for a particular time period the current density in a MTJ reaches the Critical Current Density (J_c) and the MTJ switches it's state. The switching to Parallel or Anti-parallel state depends upon the direction of current applied. While reading the data from MTJ, a current less than I_C is applied.

The STT MTJ has two advantages over other writing schemes; the first advantage is that STT switching eliminates the need for additional write lines, thereby simplifying the circuitry used to control the device. The second advantage is that STT switching is dependent on the current density [9]. A STT-MTJ is shown in Fig. 3.

3 Properties Of STT MTJ

3.1 TMR (Tunnel Magneto resistance Ratio) and its bias dependence

The MTJs exhibits a high difference in parallel and Anti-parallel resistances represented as R_P & R_{AP} respectively. This difference is due to the coherent tunneling [11]. The ratio between the two resistance values is named Tunnel Magneto resistance Ratio (TMR) and defined in Eq. (3.1). Recent research into spin-dependent tunneling in transition-metal-based MTJs has resulted in TMRs that have surpassed 500% at room temperature [12].

$$TMR = \frac{R_{AP} - R_P}{R_P} \qquad (3.1)$$

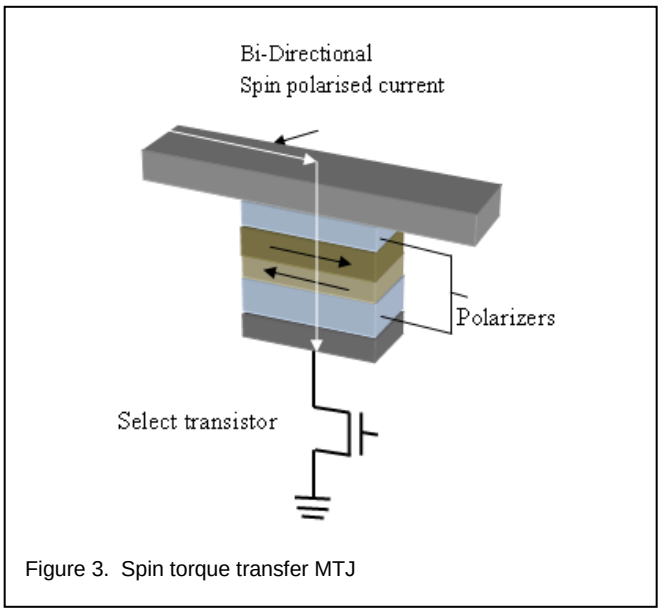

Figure 3. Spin torque transfer MTJ

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One of the properties of a MTJ is that this ratio changes with the bias voltage (v) on the MTJ. Increasing the bias causes a sharp decrease in R_P which is also asymmetric for the positive and negative bias voltages; in Anti-parallel state the resistance R_{AP} remains almost unchanged with the bias voltage. Fig. 4 shows the change in resistances with respect to bias voltages. Many mechanisms were proposed to mathematically prove this dependence but no model was able to reveal all the parameters which can give the relation between the TMR and the voltage bias.

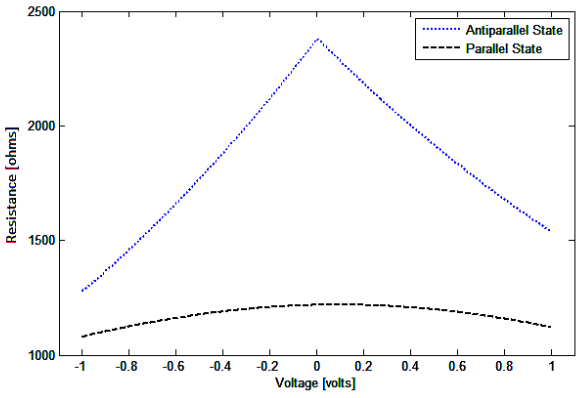

Figure 4. Voltage bias dependence of Resistance in Anti-parallel state (Upper curve), Voltage bias dependence of Resistance in Parallel state (Lower curve).

For emulating the effects of voltage bias on resistance of the MTJ. The available data from the previous models [9] & [10] is fitted using the Gaussian Function, Eq. (3.2).

$$R = a \times e^{-\left(\frac{v-b}{c}\right)^2} \qquad (3.2)$$

Where R is the resistance of MTJ and a, b and c are the fitting parameters. The complete characteristics is fitted in this equation in three separate regions that are Anti-parallel state with positive voltage bias, Anti-parallel state with negative voltage bias and parallel state. Table 1 shows the values of fitting parameters a, b and c for different regions.

TABLE 1
Values of Fitting parameters a, b and c in Parallel state, Anti-parallel state with positive bias and Anti-parallel state with negative bias.

Parameter	Parallel state	Anti-parallel state with positive bias	Anti-parallel state with negative bias
a	1219	2.832×10^9	8368
b	0.09195	-64.44	4.503
c	3.142	17.23	4.013

Substituting the values of fitting parameters from Table 1 in Eq. 3.2, R_{PS} (Resistance eqution in Parallel state), R^{+}_{APS} (Resistance equation in Anti-parallel state with positive bias) and R^{-}_{APS} (Resistance equation in Anti-parallel state with negative bias) can be formed.

3.2 Critical switching current (I_C)

This is the most important property of the MTJ as current density decides in which state (parallel or Anti-parallel) the MTJ will remain. The critical switching current (I_C) is defined as a function of switching time (τ) and operating temperature (T), as shown in Eq.3.3 [13].

$$I_C = I_{C0}\left\{1 - \left(\frac{kT}{E}\right) ln\left(\frac{\tau}{\tau_0}\right)\right\} \qquad (3.3)$$

Where τ_0 is the inverse of write attempt frequency, k is the Boltzmann constant, E is barrier height and I_{C0} critical current at zero Kelvin.

In this model the critical switching currents are calculated using Eq. 3.3 at room temperature taking the thermal stability coefficient E/kT equals to 22, with write pulse width τ equals to 10ns and inverse of write attempt frequency τ_0 equals to 1ns. The values of switching current in Parallel and Anti-parallel states were 350μA and -450μA respectively and the corresponding values of switching voltages in Parallel and Anti-parallel states were 0.425v and -0.700v respectively. The complete list of parameters used in the MTJ model is given in Table 2.

TABLE 2
MTJ Model Parameters

Parameter	Description	Value
R_p	Resistance Parallel state	1281Ω
R_{AP}	Resistance Anti-parallel state	2377Ω
TMR	Tunnel Magnetoresitance Ratio	95%
I_{c0P}	Critical switching current at zero Kelvin Parallel state	$390\mu A$
I_{c0AP}	Critical switching current at zero Kelvin Anti-parallel state	$-500\mu A$
I_{cP}	Critical switching current Parallel state	$350\mu A$
I_{cAP}	Critical switching current Anti-parallel state	$-450\mu A$
v_{cP}	Critical switching Voltage Parallel state	$425mv$
v_{cAP}	Critical switching Voltage Anti-parallel state	$-700mv$
$\frac{E}{kT}$	Thermal Stability coefficient	22

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4 Device model

An STT-MTJ can be simulated using a circuit or an HDL (Hardware Discriptive Laguage) code based on the behavioural model of STT-MTJ explained in this paper. In addition Algorithm 1 praposes an algorithm, which can be used to simulate the device using an HDL code such as Verilog-A.

Algorithm 1
For implementation of Spin Torque Transfer Magnetic Tunnel Junction (STT MTJ)

$state = parallel$
for all
do
$v \leftarrow input\ voltage$
if $state = parallel\ \&\ v \geq v_{cP}$ ***then***
$state = Antiparallel\ with + ve\ bias$
end if
if $state = Antiparallel\ with + ve\ bias\ \&\ v \leq 0$ ***then***
$state = Antiparallel\ with - ve\ bias$
end if
if $state = Antiparallel\ with - ve\ bias\ \&\ v \leq v_{cAP}$ ***then***
$state = parallel$
end if
if $state = Antiparallel\ with - ve\ bias\ \&\ v \geq 0$ ***then***
$state = Antiparallel\ with + ve\ bias$
end if
if $state = parallel$ ***then***
$R \leftarrow R_{PS}$
end if
if $state = Antiparallel\ with + ve\ bias$ ***then***
$R \leftarrow R^{+}_{APS}$
end if
if $state = Antiparallel\ with - ve\ bias$ ***then***
$R \leftarrow R^{-}_{APS}$
end if
$I \leftarrow v/R$
end for

5 Design of MTJ Based Register

MTJ is a magnetic storage device, with data being stored in the form of resistance.An MTJ centred device utilizes this property of MTJ to be used as a basic element for memories and other logic devices. This needs an interface between the MTJ and existing technolgy, so that the device can store the data on MTJ and read back when required. Here a simple interface is created using a signal conditioning circuit at the input of MTJ and an output comparator (Figure 5).

5.1 Signal conditioning circuit

The Signal conditioning circuit changes the input voltage levels from the input lines Write 1 (*wr1*), Write 0 (*wr0*) and Read (*rd*) (Figure. 5) and sets them to a level suitable for the working of MTJ. Writing the MTJ needs a high potential difference across MTJ terminals while on reading only a mild potential is required. The input voltage (v_{in}) across the MTJ is calculated using Equation.

$$v_{in} = wr1 \times 1 + wr0 \times -1 + rd \times 0.4 \quad (5.1)$$

A negative voltage is applied while reading the data from MTJ because it is difficult to switch the MTJ from its Anti-parallel state to its Parallel state. So we get a higher read margin by using the negative voltage bias, while reading.

5.2 Output Comparator

The output of signal conditioning circuit (v_{in}) is given to the MTJ in series with a 1K resister. On application of the read pulse voltage drop across MTJ (v_{MTJ}) changes as it switches from Parallel state to Anti-parallel state. This change is due to the di_erence in resistance of Parallel and Anti-parallel state. The v_{MTJ} is compared to a reference value of voltage (v_{ref}) between the two states of MTJ and corresponding voltage output (v_{out}) is given at the output terminal.

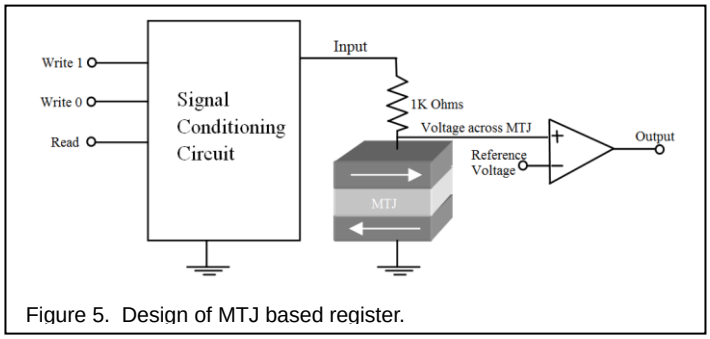

Figure 5. Design of MTJ based register.

6 Transient Simulation

The model of STT-MTJ was implemented using Verilog-A and verified using Synopsys Hspice 2010. Figure 6 shows the response of the model on application of 1.2 volts 0.05 MHz triangular wave, on the top Triangular input is shown. Middle waveform shows the variation of model resistance with the input voltage and waveform at the bottom shows the current through MTJ, slope of current changes as MTJ switches state.

A register based on STT-MTJ was also simulated, Figure 7 shows the inputs and corresponding output of signal conditioning circuit i.e. Write 0 (*wr0*), Write1 (*wr1*), Read (*rd*) and Input voltage (v_{in}). Equation 5.1 is used to calculate the value of v_{in}, as shown in the graph. Figure 8 shows the Input voltage of MTJ circuit (v_{in}) and voltage across MTJ (v_{MTJ}). Figure 8 shows the voltage across MTJ (v_{MTJ}) with -290mv reference voltage (v_{ref}) and corresponding voltage output (v_{out}). The output comes whenever the voltage across MTJ drops below -290mv.

7 Conclusion

A novel and simple model of a Spin Torque Transfer Magnetic Tunnel Junction was presented in this paper. The model accurately emulated the main characteristics of a STT-MTJ such as its TMR and the voltage dependence of its Resistance. The model can be used for faster simulations of hybrid Mag-

netic CMOS circuits such as MRAMs, nonvolatile Flip-Flops and many other related devices. The model can easily be improved to show the other properties of MTJ such as temperature dependence of the TMR and dynamic switching based on some other parameters.

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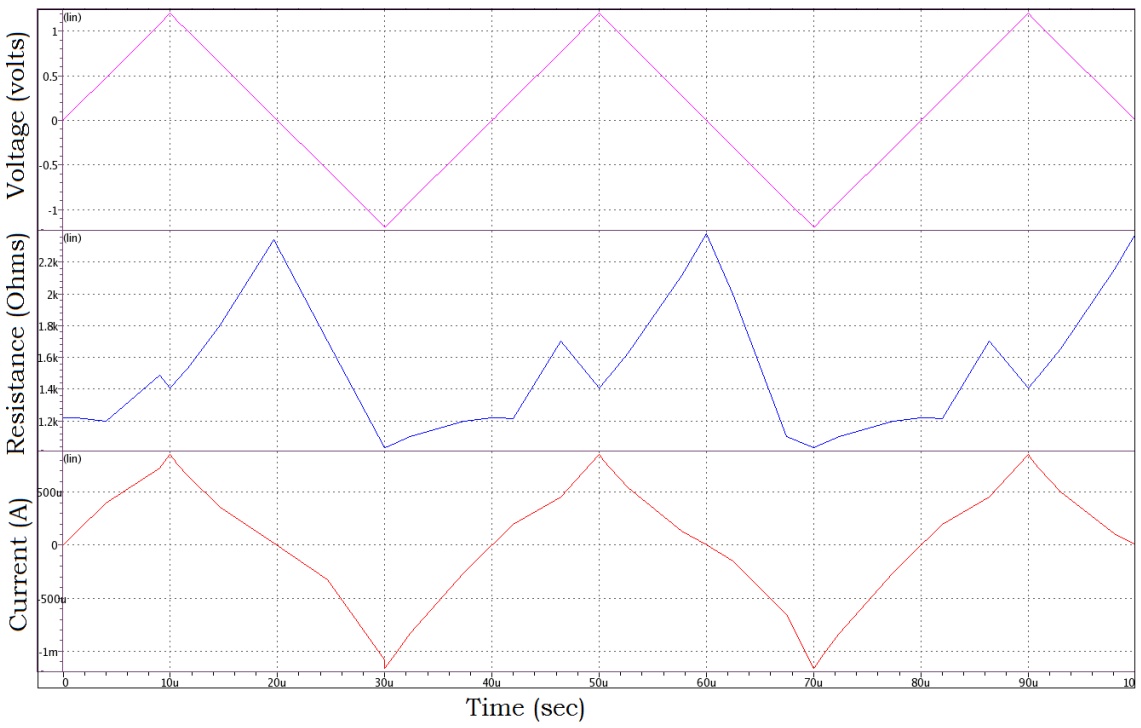

Figure 6. Transient response of Verilog-A Behavioural model of MTJ. Input triangular voltage, model resistance and current.

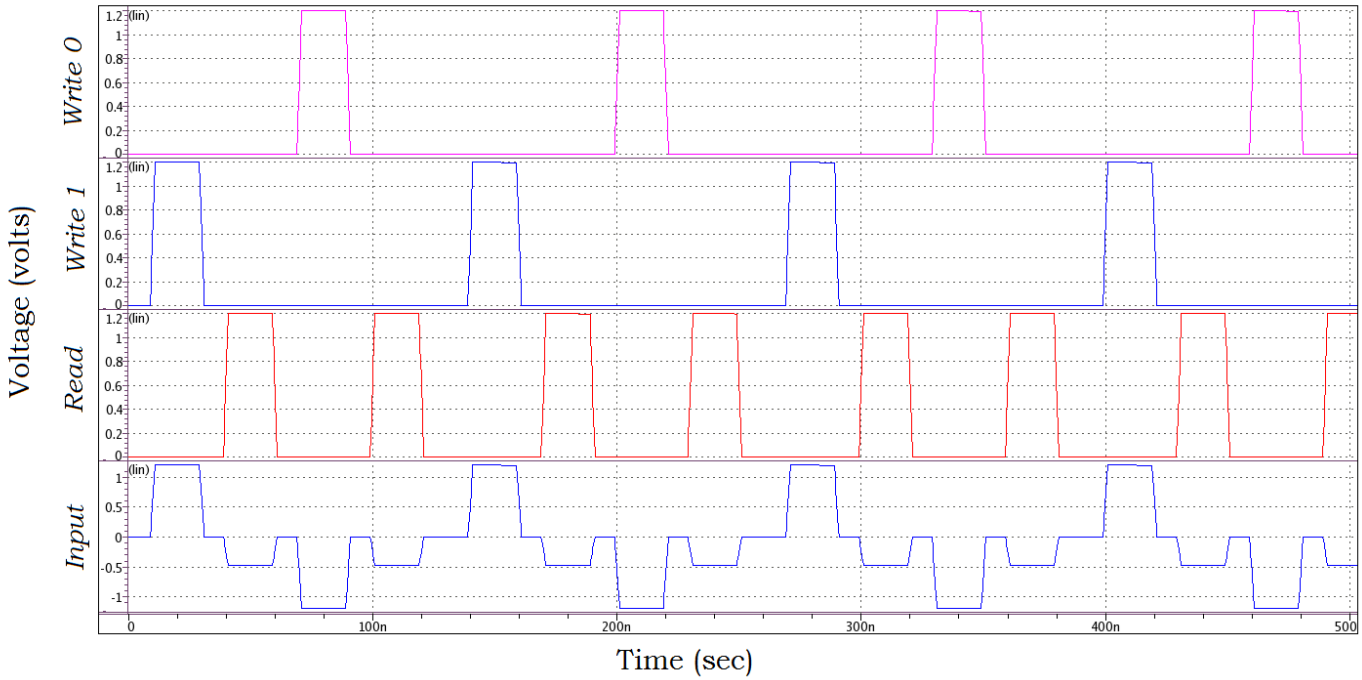

Figure 7. Inputs and corresponding output of signal conditioning circuit i.e. Write 0 (*wr0*), Write1 (*wr1*), Read (*rd*) and Input voltage (v_{in}).

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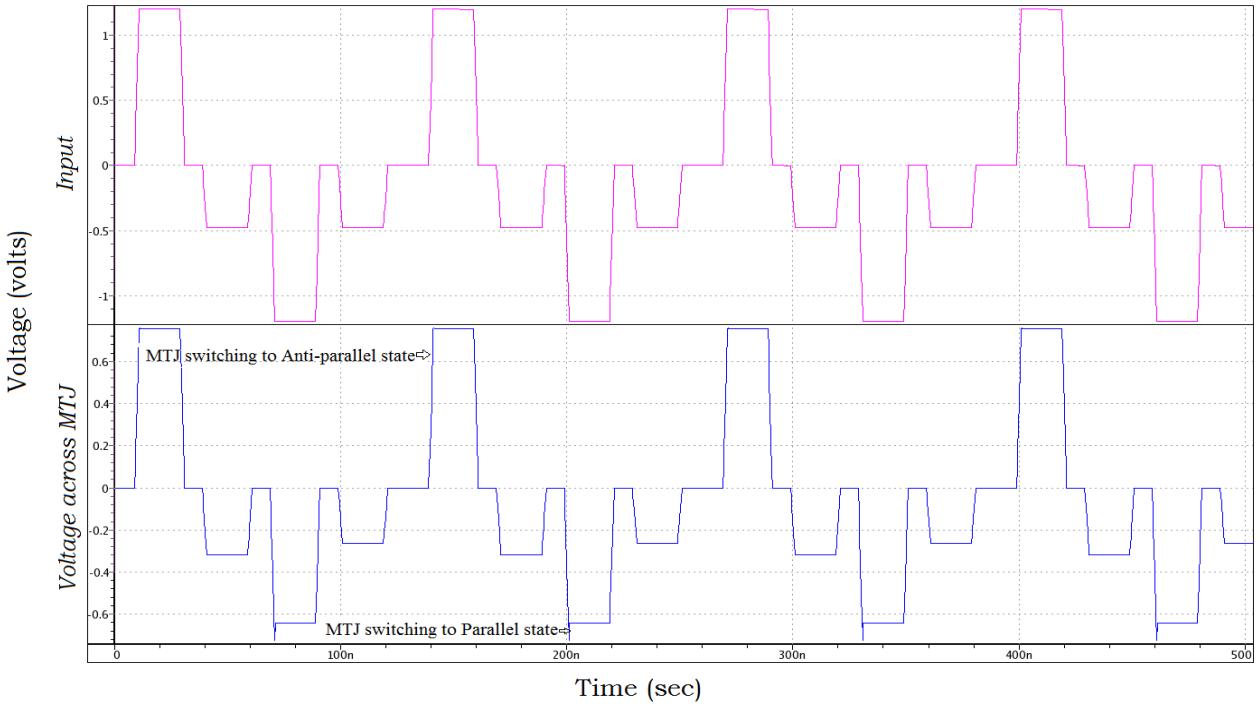

Figure 8. Input voltage of MTJ circuit (v_{in}) and voltage across MTJ (v_{MTJ}).

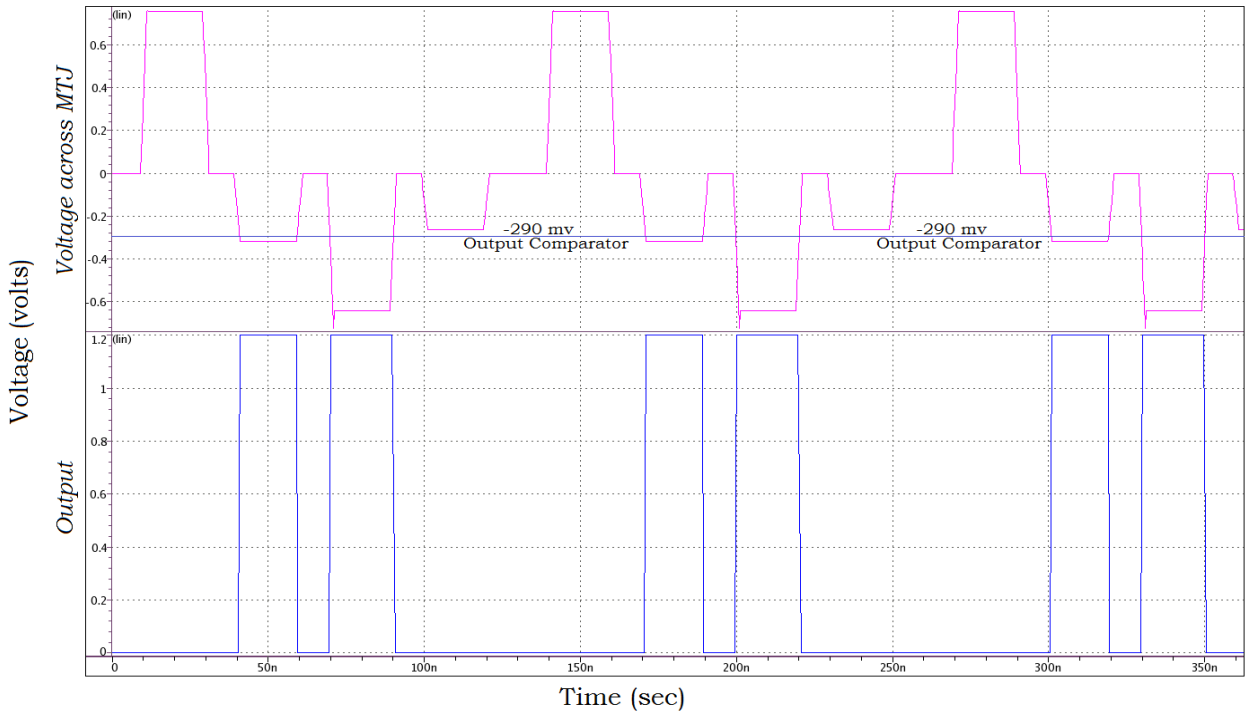

Figure 9. Voltage across MTJ (v_{MTJ}) with -290*mv* reference voltage (v_{ref}) and corresponding voltage output (v_{out}).