

An Efficient 16-Bit Multiplier based on Booth Algorithm

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ABSTRACT

Multipliers are key components of many high performance systems such as microprocessors, digital signal processors, etc. Optimizing the speed and area of the multiplier is major design issue which is usually conflicting constraint so that improving speed results mostly in bigger areas. A VHDL designed architecture based on booth multiplication algorithm is proposed which not only optimize speed but also efficient on energy use.

Keywords : VHDL; Multiplier; Booth Algorithm

1 INTRODUCTION

MULTIPLIERS are key components of many high performance systems such as microprocessors and digital signal processors etc. Generally a system's performance is determined by the performance of the multiplier because the multiplier is generally the slowest element in the system. Furthermore, it is generally the most area consuming. Hence, optimizing the speed and area of the multiplier is a major design issue. However, area and speed are usually conflicting constraints so that improving speed results mostly in larger areas [1]. As a result, a whole spectrum of multipliers with different area-speed constraints has been designed with fully parallel multipliers at one end of the spectrum and fully serial multipliers at the other end [2]. The intermediary are digit serial multipliers where single digits consisting of several bits are operated on. Genetic algorithm is used to optimize the area of multiplier [3].

Binary multiplication can be achieved in a similar fashion as to multiply decimal values. Using the long multiplication method, i.e. by multiplying each digit in turn and then adding the values together. This method have more computational cost, additionally the computation time increases with larger number. Therefore, an efficient method of binary multiplication is applicable where recursive adding of multiplicand and multiplier make sense. Different algorithms are used for multiplication of number, however, Booths Algorithm is comparatively more efficient than the other. Further, multiplication of signed number also need consideration of signed digit as multiplying numbers with the same sign produces a positive product, but multiplying a positive number by a negative number yields a negative product. The requirement is to design an 16-by-16 bit multiplier based on the shift and add method.

The multiplier shall accept as inputs of an 16-bit multiplier and 16-bit multiplicand as well as a *Start* signal. The multiplier shall then calculate the result using the shift and add method
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and provide the 16-bit result along with a *Stop* signal. The complete 16 × 16 bit Multiplier Organization as a top-level module is depicted in figure-1, which explores all the lower level functional modules [4][5].

The basic components of the multiplier are (1) Register, (2) Adder, (3) Booth Selector (MUX, Multiplexer) and (4) Encoder.

With the Introduction in section-1, an overview of VHSIC Hardware Description Language (VHDL) is summarized in section-2. Section-3 describes the steps of computation of Booth's Multiplication Algorithm. Section-4 provides the understanding of section-3 with an arithmetic multiplication example. Section-5 states the discussion and key points with conclusion. Finally, the proposed architecture and results are discussed.

2. VHDL

VHDL is a language for describing digital electronic systems. It was initially designed for United States Government's Very High Speed Integrated Circuits (VHSIC) program, initiated in 1980. Hence the VHSIC Hardware Description Language (VHDL) was developed, and subsequently adopted as a standard by the Institute of Electrical and Electronic Engineers (IEEE) in the US. VHDL is designed to fill a number of needs in the design process. Moreover it is an efficient language that allows description of the structure of a design, i.e. how base design is decomposed into sub-designs, and how those sub-designs are interconnected.

Secondly, it allows the specification of the function of designs using familiar programming language forms. Thirdly, it allows a design to be simulated before being manufactured, so that designers can quickly compare alternatives and test for correctness without the delay and expense of hardware prototyping.

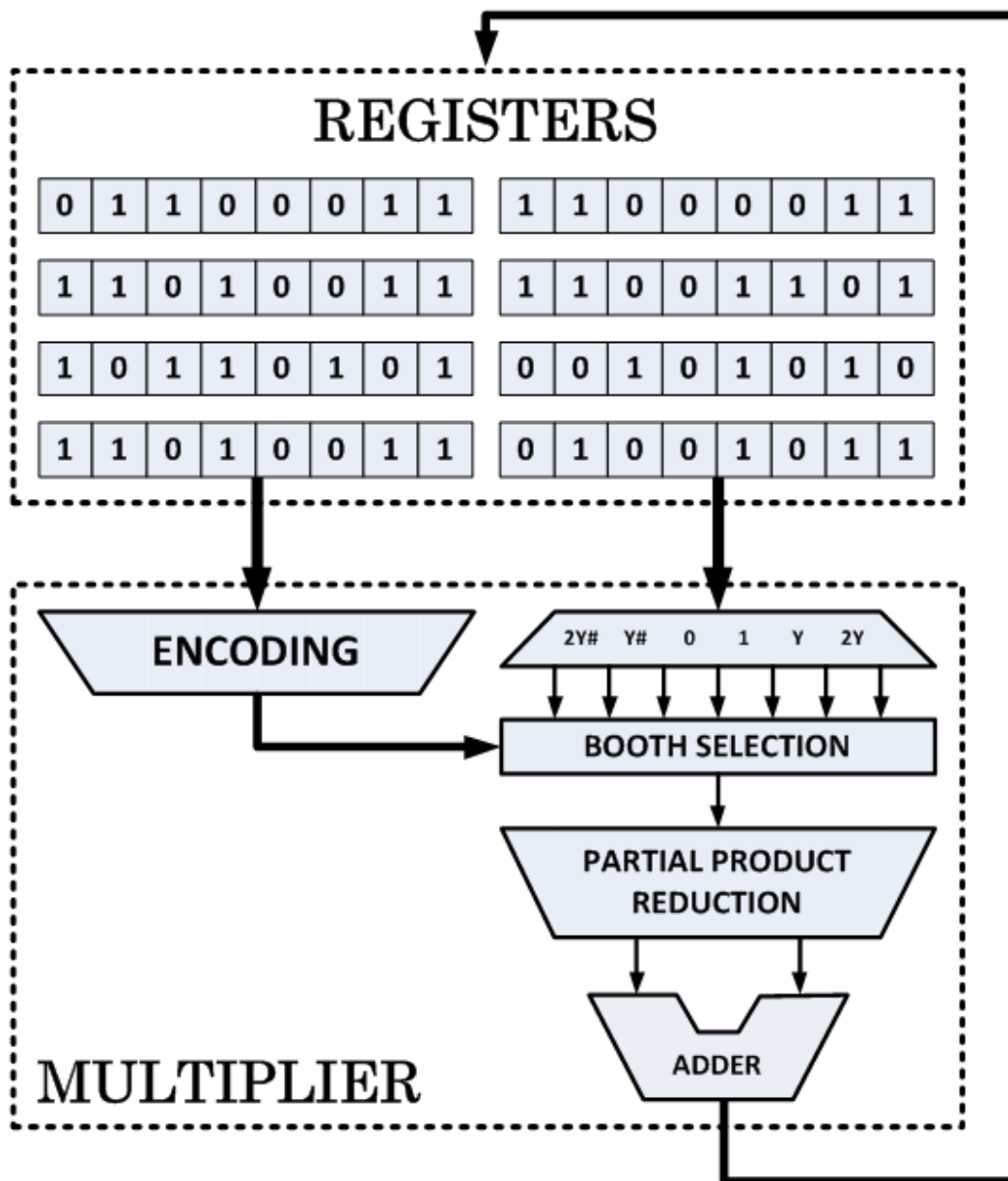


Figure-1: 16 x 16 bit Multiplier Organization

2.1 Basic Component of VHDL

VHDL have following Design Component:

- i. Describing Structure
- ii. Describing Behavior
- iii. Discrete Event Time
- iv. Modeling (Simulation)

3. BOOTH ALGORITHM

Booth's multiplication algorithm is an algorithm that multiplies two signed binary numbers in two's complement notation. The algorithm was invented by Andrew Donald Booth in 1951. Booth's algorithm involves repeatedly adding one of two pre-determined values A and S to a product P , then performing a rightward arithmetic shift on P . Let m and r be the mul-

tiplicand and multiplier, respectively; and let x and y represent the number of bits in m and r .

1. Determine the values of A and S , and the initial value of P . All of these numbers should have a length equal to $(x + y + 1)$.
 - i. A : Fill the most significant (leftmost) bits with the value of m . Fill the remaining $(y + 1)$ bits with zeros.
 - ii. S : Fill the most significant bits with the value of $(-m)$ in two's complement notation. Fill the remaining $(y + 1)$ bits with zeros.
 - iii. P : Fill the most significant x bits with zeros. To the right of this, append the value of r . Fill the least significant (rightmost) bit with a zero.
2. Determine the two least significant (rightmost) bits of P .
 - i. If they are 00, do nothing. Use P directly in the next step.

- ii. If they are 01, find the value of $P + A$. Ignore any overflow.
 - iii. If they are 10, find the value of $P + S$. Ignore any overflow.
 - iv. If they are 11, do nothing. Use P directly in the next step.
3. Arithmetically shift the value obtained in the 2nd step by a single place to the right. Let P now equal this new value.
4. Repeat steps 2 and 3 until they have been done y times.
5. Drop the least significant (rightmost) bit from P . This is the product of m and r .

4. EXAMPLE

Find the value of $(-3) \times 2$ in decimal system?

Let $m = -3$ and $r = 2$, and $x = 4$ and $y = 4$:

- i. $m = 1101$
- ii. $m' = 0011$ (2s Complement of m)
- iii. $r = 0010$

Therefore,

- i. $A = 1101\ 0000\ 0$
- ii. $S = 0011\ 0000\ 0$
- iii. $P = 0000\ 0010\ 0$

Perform the loop four times:

- 1) $P = 0000\ 0010\ 0$. The last two bits are 00.
 $P = 0000\ 0001\ 0$. Do nothing, Arithmetic right shift.
- 2) $P = 0000\ 0001\ 0$. The last two bits are 10.
 $P = 0011\ 0001\ 0$. $P = P + S$.
 $P = 0001\ 1000\ 1$. Arithmetic right shift.
- 3) $P = 0001\ 1000\ 1$. The last two bits are 01.
 $P = 1110\ 1000\ 1$. $P = P + A$.
 $P = 1111\ 0100\ 0$. Arithmetic right shift.
- 4) $P = 1111\ 0100\ 0$. The last two bits are 00.
 $P = 1111\ 1010\ 0$. Do nothing, Arithmetic right shift.

Drop the least significant (rightmost) bit from P . We obtained 1111 1010. This is the product of $(-3) \times 2$, which is equivalent to -6 decimal. [6].

5. DISCUSSION

The power consumption in VLSI circuit is dependent on gate switching activity which consequently depends upon design. Booth Algorithm provides a simpler design. Even in case of large dimension of data, gate switching is controlled. Therefore using Booth Algorithm and Modified Booth Algorithm may reduce power consumption as consequence of data complexity [7][8]. It is found that in multiplier circuit, Modified Booth Algorithm reduces power consumption as compared to other methods of multiplication.

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