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A LOW POWER CMOS ELECTROCARDIOGRAM AMPLIFIER DESIGN USING 0.18µM CMOS TECHNOLOGY

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ABSTRACT

An electrocardiogram (ECG) amplifier was designed in 0.18 µm standard CMOS technology with the power consumption of 1.47µw, 54.5 $pV/\sqrt{Hz}$ input-referred noise, and a common-mode rejection ratio of 82 dB. The ECG amplifier was designed that pick-up the lower power signal from the heart. The main challenge includes amplifying the weak signal in the presence of noise. The OTA design is well utilized to remove the flicker noise. The performance of the ECG amplifier can be improved by input transistor sizing, device matching and gain-setting adaptive element. Compared to previous work [1], the signal quality is better with less power consumption. The amplified signal can be processed and send to the hospital via wireless transceiver.

1 INTRODUCTION

Recently, the most of ECG measurement are portable due to its small size and power consumption. ECG amplifiers are battery powered devices due to its wearable condition. Normally, electrocardiogram (ECG) measurement setup consists of electrodes to measure the ECG signal from the human body, an analog front end (AFE) amplifier that amplifies the ECG signal, analog to digital converter (ADC) for digitizing the analog ECG signal, and a display device to monitor the patient's heart regularly.

The ECG system is portable in the sense, it probably consist of wireless transceiver in the system. The wireless link is connected between the ADC unit and display unit [2], [3]. The universal connectivity allows the system to connect it to wide range of area. The analog-to-digital conversion is done for the biomedical signals less than 1µw and the ADC consumes only less power [4], [5]. Design of analog front end (AFE) amplifier mainly focused on power consumption and noise [6] – [10]. The use of feedback loop technique eliminates $1/f$ noise and maintains CMRR to the allowable level.

Fig.1 shows [1] the block diagram of electrocardiogram (ECG) amplifier. The ECG signal is collected by the pair of electrodes connected in the human body at two locations. The location may be left arm and right arm. The electrode may pick-up a considerable amount of an interfering common -mode 60-Hz signal. The $V_{60\,Hz}$ signal is nearly available at all location on the human body. The active grounding is connected to remove the $V_{60\,Hz}$ noise and it allows higher gain [11], [12].

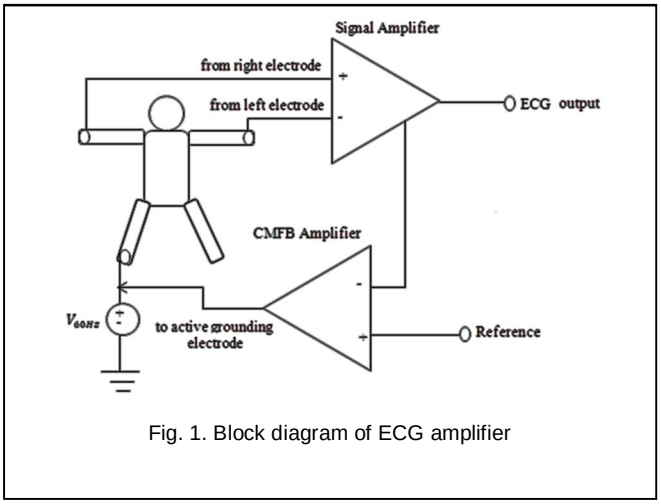

Fig. 1. Block diagram of ECG amplifier

The third reference electrode is used to drive the common mode value that yields better performance for measuring ECG signal. Active grounding with common-mode feedback amplifier (CMFB) is used in the ECG system as described in [11]. This paper is organized as follows: In section II, the design of ECG amplifier is presented. In section III, the common mode rejection ratio and its noise are analyzed. In section IV, the measured performance of the electrocardiogram amplifier is presented. In section V,

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the summary of electrocardiogram amplifier compared with the previous work is concluded.

2 ECG AMPLIFIER DESIGN

The amplifier is designed in 0.18 µm standard CMOS technology. To bias all the devices, the current reference is used [13]. Because of NMOS current mirror circuit, current flowing through the circuit depends on the V_{dd}. Additionally, we work with the power supply of 1V.

2.1 Instrumentation-Amplifier Design

The design of the analog front end amplifier (AFE) is a two-stage instrumentation amplifier as shown in the Fig.2. The ECG signal obtained from the electrode is too small which is less than 1µv and contains lot of noise. It is

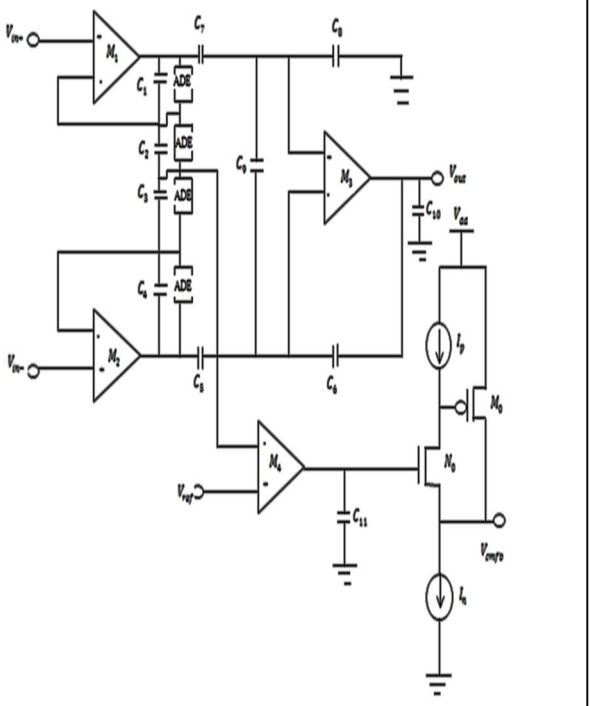

Fig. 2. ECG schematic

necessary to amplify the weak signal and filter the noise present in the signal. The following reason describes the usage of instrumentation amplifier.

a) High gain.
b) High common-mode rejection ratio (CMRR)
c) High input impedance.
d) High common-mode extraction.

The gain requirement can be reduced by spreading the amplification between two stages and it provides the necessary gain. The instrumentation amplifier boosts CMRR [14]. The common-mode extraction is done by the common-mode feedback amplifier. The instrumentation amplifier offers excellent accuracy and more flexibility. The flexible 3-opamp design and small size allows us to use in wide range of application.

2.2 OTA Design

The operational transconductance amplifier (OTA) is the basic block of instrumentation amplifier used in the ECG amplifier shown in the Fig. 3. The OTA design was implemented as long tailed pairs with current mirror circuit. Here, PMOS devices are preferred compared to NMOS devices because of less flicker noise [15] in PMOS devices. To reduce the flicker noise, we should increase the W/L ratio of input transistor in the first stage of the amplifier. The device matching in the second stage of the amplifier does not provide any change in the noise performance.

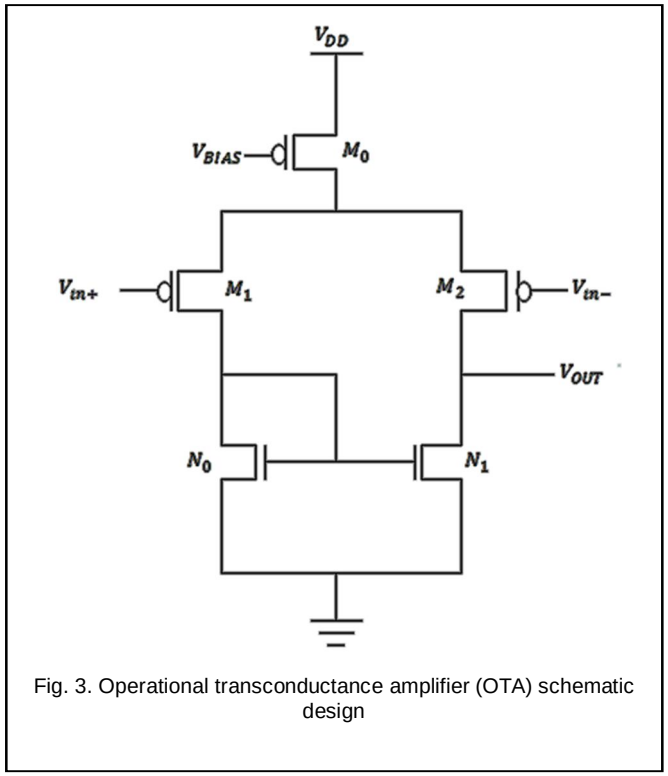

Fig. 3. Operational transconductance amplifier (OTA) schematic design

2.3 Adaptive Element-Based Amplification

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The previous ECG amplifier [1] uses ratio of resistor to set the gain values. But, the resistors introduce noise and it has poor matching property. Hence, the capacitors are used to set the gain to ECG amplifier [16]. Along with capacitors, metal oxide semiconductors (MOS) bipolar pseudo-resistors are used as the adaptive element to set the gain very effectively [17], [18].

2.4 Common-Mode Feedback Amplifier

The common-mode feedback amplifier topology is used to reject noise from common-mode amplifier. The amplifier is connected with reference voltage to drive relatively low impedance. The voltage buffer is required in between the operational transconductance amplifier and the reference electrode. In the voltage buffer, 0.3-0.5µA bias current is required to eliminate the interference from the common mode signal. Along with that, we used source follower circuit.

3 CMRR & NOISE ANALYSIS

The presence of 60-Hz hum in ECG signal made the necessity of common-mode rejection in the noise performance. The CMRR value can be obtained by

$$CMRR \text{ in } \% = 20 \log \frac{A_{diff}}{A_{com}} \quad (1)$$

The overall differential gain of the amplifier is given by

$$A_{diff} = A_{1st\,stage} + A_{2nd\,stage} \quad (2)$$

Normally, the gain the amplifier is given by output voltage divided by the input voltage. Here, the capacitor based amplification is done to set the gain of the amplifier. The common-mode gain A_{com} is calculated from the closed loop gain of the feedback amplifier can only be determined by capacitors.

$$A_{com} = \frac{C_2}{C_2 + C_3} \quad (3)$$

The total noise power at the output of an OTA can be calculated by summing the noise current power from each transistor. The transistor, which produce current noise power given by [19]

$$|\overline{i_n}| = \frac{8}{3} kTg_m\Delta f \quad (4)$$

The total noise power from single OTA is calculated by adding the noise power from each transistor. The total input-referred noise can be given by adding the noise power from each OTA circuit.

4 RESULTS & DISCUSSION

The simulation software used for designing the amplifier is cadence virtuoso analog design environment. The amplifier circuit designed is shown in the Fig 4. The power is supplied by independent voltage sources which is 1v. Input voltage is chosen as 1µV sine wave signal for simulation purpose and the amplifier produces the non-linear amplified output which is shown in the Fig 5. The AFE amplifier consumes 1.47µW of power. The gain and bandwidth are measured by connecting the one terminal to the output and another to the input of the amplifier. The measured gain and bandwidth, at 44.2dB and 21Hz, were seen in the Fig 6. To measure CMRR, the inputs are connected together and it is then connected to the CMFB output by resistors R_{CM} andR_{CMFB}. The measured CMRR value is 82dB. To measure noise, the inputs are connected together and the noise for each OTA is measured and the total noise from each OTA is calculated is found to be 54.5pV/$\sqrt{Hz}$.

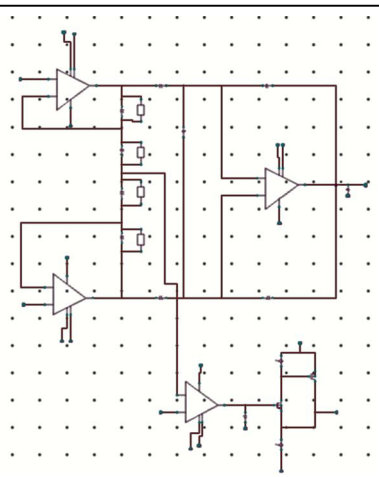

Fig. 4. ECG schematic in virtuoso analog design environment

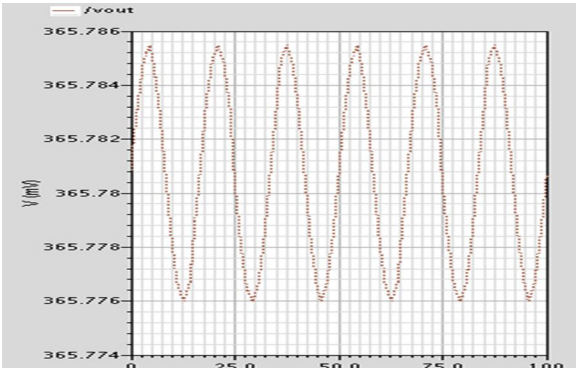

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TABLE 1
ECG PERFORMANCE

Power	1.47µW
Gain	44.23dB
Bandwidth	21Hz
Noise	54.5pV/$\sqrt{Hz}$
CMRR at 60Hz	82.3dB

Statements that serve as captions for the entire table do not need footnote letters.
W = watts, Hz = hertz, dB = decibels, V = volt.

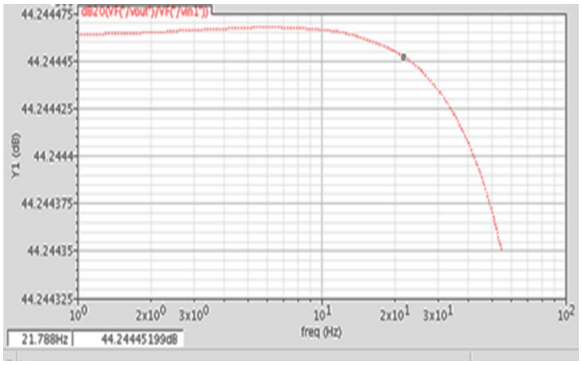

Fig. 6. The measured frequency response of the amplifier

Table I shows the overall experimental result of the electrocardiogram (ECG) amplifier.

5 CONCLUSION

The ECG amplifier is designed with 54.5pV/$\sqrt{Hz}$ of input-referred noise, 82 dB CMRR, and 1.47µW power consumption. These performance factors provide the instrumentation amplifier as low noise and low power device with common-mode feedback. The instrumentation amplifier can be widely used in wireless, battery enabled ECG monitoring applications.

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